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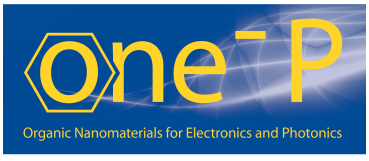

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Contents

Introduction

1

1.1 General Introduction

The field-effect transistor (FET) is the basic building block for solid-state electronics. A FET acts as a micro-electronic switch: the electrical resistance between two electrodes depends on the voltage applied to a third electrode. The source and drain electrodes are connected to a semiconductor, as illustrated in **Fig. 1.1a**. The third electrode is called the gate and is electrically insulated from the semiconductor.

Electronic circuits are made by combining many transistors. In our every-day life we find electronic circuits everywhere, in our phone or computer, but also in a bicycle light or washing machine. Conventionally, inorganic materials such as germanium and silicon are used for semiconductor devices and circuits. They are robust and can be patterned to form extremely small devices, but they are also expensive and brittle. Organic electronics on the other hand is based on organic, carbon-based, semiconductors. The properties of organic materials can be tuned with chemistry, opening a whole new range of possibilities for applications and science. Organic materials can for example be designed to be flexible or soluble in solvents, which allows for flexible electronics and 'ink-based' processing techniques. Opto-electronic properties such as the bandgap can be tuned as well. Additionally, when produced in high volumes, production costs are possibly low.

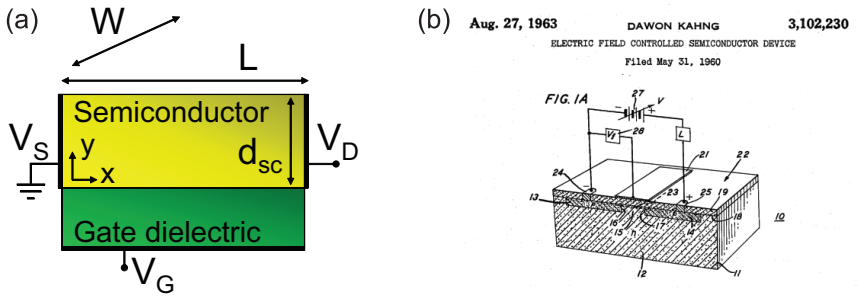

Figure 1.1. (a) Schematic representation of a field-effect transistor. The semiconductor thickness, width and length are indicated, as well as the source, drain and gate biases. (b) The first report of a metal-oxide-semiconductor based transistor [1].

A detailed understanding of the charge transport is essential in order to develop new organic semiconductors and devices. A transistor is a convenient device to study the charge transport. In this thesis, the impact on the charge transport of several recently demonstrated organic transistor structures is studied. The transistors were fabricated and measured, and two-dimensional (2D) calculations are used as a tool to study the transport in different transistor geometries.

This chapter serves as an introduction into organic electronics. To begin with, a historical perspective will be presented, from the discovery of semiconductors to state of the art organic circuits. Next, the charge transport mechanisms in organic semiconductors are discussed. Then, the basic layout and operation of organic transistors, dual-gate transistors and organic memory are introduced. Finally, an outline of this thesis is presented.

1.2 History of transistors and circuits

Inorganic electronics

The history of semiconductor devices starts in 1833, when Michael Faraday observed that the electrical conductivity of silver sulfide increases with increasing temperature [2]. This is a typical effect of semiconductors, and it is opposite to what is measured in metals, where conductivity decreases with increasing temperature. The first idea of the transistor was born in 1926, when Julius Lilienfeld filed a patent on a 'Device for controlling electric current' [3]. In this patent he described a three-electrode amplifying semiconductor device [4]. There is however no proof that Lilienfeld made actual working prototypes. It took until after World War II for the first working transistor to be fabricated. In 1948, John Bardeen and Walter Brattain invented the point-contact transistor at Bell Laboratories [5]. For this important discovery they received, together with William Shockley, the Nobel prize in physics in 1956 [6]. A next breakthrough can be considered the first successful demonstration of a metal-oxide-semiconductor (MOS) FET in 1960, also at Bell Labs [1]. In the MOS design, the gate is electrically insulated from the semiconductor, as illustrated in Fig. 1.1b. The majority of transistors produced today are MOSFETs, and also the organic transistors used in this thesis are based on the MOS concept.

One of the inventors of the MOSFET, Dawon Kahng, realized its potential ease of fabrication and the possibility of application in integrated circuits (ICs). The latter, building ICs from transistors and other components, appeared to be a major step forward. A key researcher was Jack Kilby, who received the Nobel prize in physics in 2000, for his work on ICs at Texas instruments [7]. The first ICs were fabricated in the '50s and '60s, and the first applications were in military and aerospace systems. For most applications, transistors were superior to vacuum tubes in terms of costs, performance, reliability and size, and transistors could now easily be integrated. Therefore ICs have a large advantage over discrete circuits, assembled from separate parts, and since the '60s steady progress has been made in the fabrication of ICs. The main focus was on making the transistor structures smaller, increasing the transistor density on an IC. In doing so, for example the processing power or memory of a single IC can be tremendously increased. To get an idea of this miniaturization: the traditional switching element, a vacuum tube is several centimeters in size. The size of a transistor made with a modern semiconductor manufacturing process is about 50 nm, a factor of 1 million smaller [8]. If we imagine a transistor on a modern PC processor to be the size of a football, the size of a vacuum tube is about the distance Groningen–Eindhoven. This distance is about three hours by car. A commercial laptop computer processor features over 1 billion transistors on a few square cm [9]. With the same football–transistor scaling factor, imagine placing 1 billion footballs accurately and consistently over an area of 35×35 km. The technological achievements to fabricate such ICs are the result of more than 60 years of enormous industrial and scientific effort.

Organic electronics

Conventional electronics is based on inorganic semiconductors such as germanium and silicon. Organic materials such as plastics are usually associated with electrical insulation. For example, plastics are used to prevent short circuit between electrical components, or to avoid electrical shocks by insulating power cables. However, in the 1950s it was discovered that some organic materials could carry an electric current [10–12]. Organic conductive materials were developed for use in xerographic applications (photocopiers) [13]. An important discovery was made in 1977, when Alan Heeger, Alan MacDiarmid, and Hideki Shirakawa found that the electrical conductivity of a polymer semiconductor could be tuned over 7 orders of magnitude [14]. This discovery was later awarded the Nobel prize in chemistry [15], and is often recognized as the start of 'organic electronics'. In the '80s, the first field-effect transistors based on a polymer semiconductor were presented [16–18]. Also, electroluminescence from organic materials such as polymer poly(p-phenylene vinylene) (PPV) was reported [19, 20],forming the basis of research on organic light-emitting diodes (OLEDs) [21, 22]. A few years later, organic semiconductors were successfully applied in solar cells [23, 24].

The realization that polymers can be used as active material in opto-electronic applications initiated substantial effort in the scientific community to explore new materials. The properties of polymer semiconductors, or organic materials in general, can be tuned by changing their chemical composition. Mechanical properties as well as opto-electronic properties can be adjusted, opening an enormous amount of possibilities for new materials. Polymers can be made strong, flexible, lightweight and can be mass produced. Polymers can be processed at low temperatures, typically below 150 °C, creating the opportunity to use a range of plastic substrates instead of glass. Many polymers are soluble in organic solvents, making it possible to create electronically active 'inks' [25]. Conventional solution processing techniques such as inkjet printing [26] or spin-coating can be employed to fabricate organic electronic circuits. Also more exotic methods [27] such as microcontact printing [28, 29] or self-assembly [30–33] are being explored. The advantages of solution processing on large areas, tunability of the material properties, and low temperature processing make organic electronics a viable candidate for flexible electronics. In addition, by producing materials on a large scale and using simple high-volume fabrication techniques, a cost advantage can be achieved.

The ultimate goal is a roll-to-roll solution-based process to fabricate ultra-low-cost flexible electronics. A proof of principle of many exciting ideas has been presented, bringing commercial application in sight. Examples of innovative new products based on flexible electronics are non-contact radio frequency identification (RFID) tags, sensors [36] and flexible displays [37–40]. A full-color flexible OLED display is shown in **Fig. 1.2a**. Recently, even a flexible organic microprocessor was realized, employing more than 3000 transistors, as shown in Fig. 1.2b [35]. Nowadays, RFID tags are used in identifying applications such as tracking pallets in warehouses for improved logistics, or recording individual finishing times in running events. A huge market is foreseen for extremely low-cost printed organic RFID tags, so-called electronic barcodes, for item-level identification. For most commercial applications the tags need to be able to store and send a unique amount of

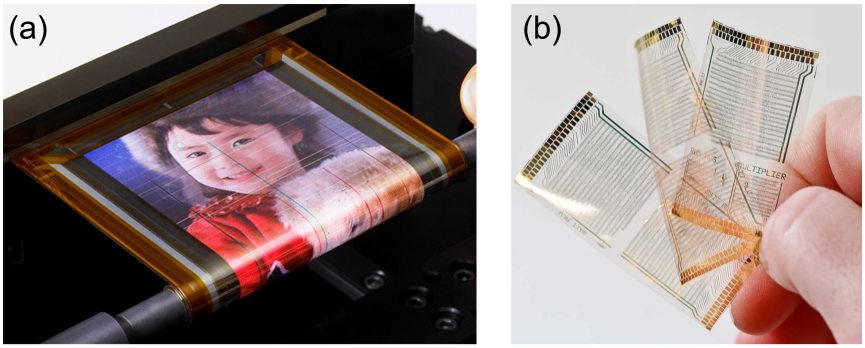

Figure 1.2. (a) Photograph of a state of the art full-color active-matrix OLED display prototype, driven by organic transistors, by Sony [34]. (b) A photograph of complex organic circuits on a flexible foil. The leftmost foils each have two microprocessors, each one is about 2×1.7 cm and contains 3381 organic transistors [35]

data of about 100 bits. Flexible, organic multi-bit RFID transponders have been realized, which were energized and read out at 13.56 MHz, the de facto standard frequency for item-level identification [41–44]. The digital code was stored in a hardwired memory [44, 45]. This type of memory cannot be reprogrammed, so it is not suitable for applications that need to be able to adjust the stored information, e.g., applications that require a book-keeping capability. For real-world applications, a non-volatile and rewritable memory technology is therefore desirable, because such technology is more universally applicable. Various organic electronics based memory technologies are being investigated, such as technologies based on metal/organic semiconductor/metal junctions [46–48], charge-trapping effects in transistors [49], and electromechanical switches [50]. Particularly, ferroelectric polymers offer promising possibilities for memories, based on both ferroelectric transistors and on ferroelectric/semiconductor bistable diodes [51–54]. Ferroelectric memories are non-volatile, rewriteable, and can be read out in a non-destructive way. By combining organic circuit technology with for example a ferroelectric memory, commercial item-level identification with organic RFID tags should be feasible in the near future.

The first commercial products making use of organic semiconductors are on the market. The main application is in OLED displays, where each pixel consists of three colored OLEDs. Small displays for cell phones are produced in enormous volumes. Over the last few years, the screen sizes has increased markedly: The first active-matrix OLED television, released on the market in 2008, had an 11 inch display [55]. For 2012, OLED televisions are announced with a screen size of 55 inch [56, 57]. All commercial applications up to now are mechanically rigid, and the displays rely on inorganic transistors in the pixel engine circuits. For fully flexible displays, all the components of the display, including the transistors driving the pixels, need to be flexible. Organic transistors are promising, but commercial introduction of organic active-matrix displays is still hampered by the poor stability and relatively low mobility of the organic semiconductors.

1.3 Charge transport in organic semiconductors

Molecular structure

Organic compounds, in a chemical sense, are compounds mainly consisting of carbon. All life on earth is based on organic matter. A carbon atom has four valence electrons, each able to form a covalent bond with other atoms. Carbon can form single, double and triple bonds. Apart from carbon, an organic molecule can contain other elements, primarily hydrogen, nitrogen, and oxygen, but also elements such as halogens or sulfur. Isolated carbon atoms contain four valence electrons, two in the so-called 2s and two in the 2p atomic orbitals. Bonds are formed by hybridizing the atomic orbitals to form new molecular orbitals. The atomic and molecular orbitals can be derived using quantum mechanical calculations, and are a representation of the volume in space where the electrons are most likely to be found. The molecular orbitals have a shifted energy with respect to the original atomic orbitals. A bond is stable if the electrons occupying a molecular orbital have a lower energy than they had before forming the bond. Combining n atomic orbitals results in n new molecular orbitals. The molecular orbitals are filled with electrons from low to high energy. In the ground state, up to a certain orbital, the orbitals contain two electrons each, while the higher energy orbitals are empty. The energetic separation between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) is called the bandgap, in analogy with the bandgap in crystalline inorganic semiconductors.

The simplest organic molecules are alkanes, linear chains of carbon atoms connected with single bonds and supplemented with hydrogen atoms. For each carbon atom in an alkane, one 2s and three 2p orbitals hybridize to form four new sp^3-orbitals. The sp^3 orbitals form four covalent σ-bonds. The electrons in a σ-bond are localized in space. The bonding in such a system results in a large bandgap, and therefore alkanes are insulators.

The electrical conductivity in organic semiconductors originates from conjugation, which is the presence of alternating single and double bonds between subsequent carbon atoms. The simplest conjugated polymer is polyacetylene, as shown in **Fig. 1.3**. In a conjugated molecule, the atomic orbitals of carbon are not sp^3 hybridized as they are in alkanes. Instead, double bonds between two carbon atoms are formed by hybridization of one 2s and two 2p atomic orbitals. The result of this so called sp^2-hybridizing is three new molecular orbitals, which form three coplanar σ-bonds. In the case of polyacetylene, each carbon atom is attached to two other carbon atoms and one hydrogen atom by a σ-bond, as shown in Fig. 1.3. The remaining fourth valence electron occupies an orbital perpendicular to the plain of the σ-bonds, called a p_z orbital. This p_z orbital overlaps with the p_z orbital of a neighboring carbon atom to form a π-bond, as illustrated in Fig. 1.3b. The σ-bond and the π-bond together make up the double bond. In contrast to a σ-bond, the electrons in a π-bond are delocalized in space. In a conjugated polymer, the delocalization is not limited to two carbon atoms, but the π-electrons are shared over the whole conjugated path. Due to the delocalization, the bandgap of a conjugated molecule is relatively small, and decreases with increasing conjugation length. However, Peierls distortion prevents the bandgap from vanishing completely, and

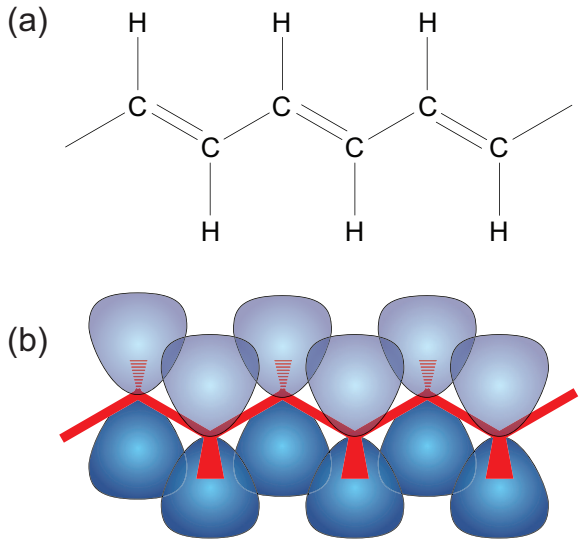

Figure 1.3. (a) Molecular structure of the simplest conjugated polymer, polyacetylene. (b) Schematic representation of the molecular orbitals in polyacetylene. The σ-bonds are indicated in red and are coplanar. The remaining p_z orbitals are perpendicular to the σ-bonds and are indicated in blue, forming a delocalized π-system.

the conjugated molecule always remains a semiconductor [58].

In a real conjugated polymer, the length of conjugated segments along a polymer chain is limited to a few nanometers, due to chemical or structural defects. Each segment differs in length as illustrated in **Fig. 1.4a** and has therefore a slightly different bandgap [59]. This structural disorder therefor leads to energetic disorder. A spatial distribution of segments with a different bandgap results in a broadening of the HOMO and LUMO levels and localization of charge carriers.

Charge transport

Early electrical measurements on disordered photoconductors showed that the carrier mobility was dependent on temperature and the applied electric field [60]. Due to the energetic disorder, the charge transport in organic semiconductors cannot be described by band transport, typical for crystalline inorganic semiconductors. In this section, the consequences of disorder on the electrical conduction will be addressed.

Crystalline semiconductors, such as silicon or germanium, have a three-dimensional (3D) lattice which is characterized by long range order. Electrons have a relatively long mean free path length and the charge transport is described by band transport. The main limiting factor for this type of transport is scattering of charges by phonons: moving electrons are hindered by thermal lattice vibrations. As the number of phonons decreases at lower temperatures, the mobility of the charge carriers increases with decreasing temperature [61].

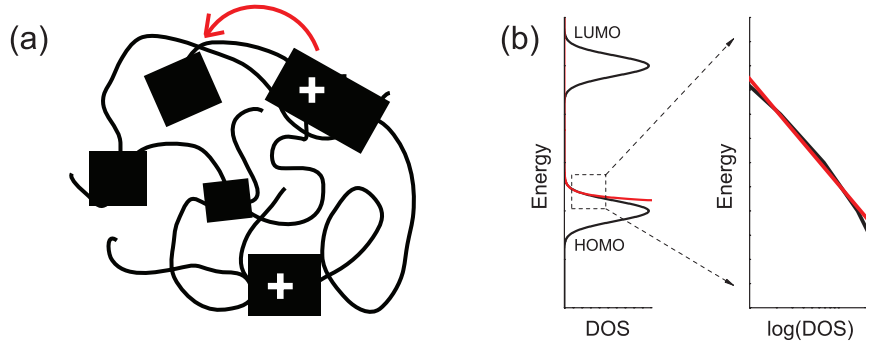

Figure 1.4. (a) Schematic picture of an amorphous polymer semiconductor. The polymer chains are broken up in conjugated segments. Charges (+) are localized and hop from segment to segment. (b) Schematic graph showing the broadening of HOMO and LUMO levels due to the energetic and structural disorder. A range of a Gaussian density of states (DOS) (black line) can be approximated by an exponential DOS (red line).

In conjugated polymers, and most organic semiconductors in general, charges are localized due to the energetic disorder. Although the charge is delocalized over a conjugated segment, these segments are limited in size. The movement of charges in the material is limited by the jumps from segment to segment, as illustrated in Fig. 1.4a. The charge transport is typically described by hopping: phonon-assisted tunneling from site to site. By absorbing a phonon, a charge carrier can gain enough energy to make a jump. Consequently, the carrier mobility increases with increasing temperature.

Many hopping models are based on a hopping rate proposed by Miller and Abrahams [62, 63]. The rate for a charge carrier hopping from site i to an unoccupied site j, W_{ij}, depends on the spatial distance, R_{ij}, and the energetic difference between the sites, $\Delta\epsilon = \epsilon_j - \epsilon_i$, and was calculated as:

$$W_{ij} = \upsilon_0 \exp(-2\alpha R_{ij}) \begin{cases} \exp\left(-\frac{\Delta\epsilon}{k_B T}\right) & \text{if } \Delta\epsilon > 0 \\ 1 & \text{if } \Delta\epsilon \leqslant 0 \end{cases} \tag{1.1}$$

where υ_0 is the attempt-to-jump frequency, α^{-1} is an effective overlap parameter, k_B is the Boltzmann constant, and T is the temperature. The left exponential term represents the tunneling probability, resulting in an exponential decrease of the rate with hopping distance. The right exponential term accounts for the phonon density. When the unoccupied site is lower in energy, this term is unity, otherwise the hop is thermally assisted.

In the pioneering work of Bässler, a charge transport model for disordered organic systems was proposed, based on hopping in a system with spatial and energetic disorder [64]. The hopping rate was assumed to follow Eq. 1.1. To describe the broadening of the HOMO and LUMO levels, a Gaussian density of states (DOS) was taken, as illustrated in Fig. 1.4b. The choice for a Gaussian DOS is supported

by the observation of Gaussian shaped optical spectra [64]. The transport in such a system cannot be solved analytically, and therefore Monte Carlo simulations were employed. The result was an expression for the carrier mobility as a function of temperature and electric field. A broader density of states leads to lower mobilities and a stronger temperature dependence. Experimental results could be described well, but only at high electric fields. By taking correlations between site energies into account, the agreement with experiments could be improved [65].

For typical semiconducting polymers the mobility extracted experimentally from diodes is low and independent of carrier density. The mobility extracted from field-effect transistors is higher and increases with charge carrier density. The carrier density in diodes is typically four orders of magnitude lower than the density found in transistors [66]. It was recognized that the mobility difference originates from the fact that the mobility has an important dependency on carrier density, apart from a dependency on temperature and field [66–69].

Vissenberg and Matters developed a model to describe the temperature and carrier density dependencies of the mobility in amorphous organic field-effect transistors [70]. Their approach is based on percolation theory and variable range hopping in an exponential DOS of localized states. Variable range hopping takes into account that it can be energetically favorable to hop over a longer distance with a low energy difference between sites, than over a shorter distance with a higher energy difference. The occupation probabilities of the initial and final states, as given by Fermi-Dirac statistics, were properly taken into account. For a Gaussian DOS, assumed previously, the problem can only be solved numerically. However, the charge transport takes place in the tail of the Gaussian DOS, which can be approximated by an exponential distribution, as illustrated in Fig. 1.4b. Using an exponential DOS, an analytical expression for the field-effect mobility of holes in an amorphous organic semiconductor was derived as [70]:

$$\mu_p = f p^{\frac{T_0}{T}-1} \tag{1.2}$$

where p is the hole density and f is a temperature dependent prefactor given by:

$$f = \frac{\sigma_0}{e}\left[\frac{\left(\frac{T_0}{T}\right)^4 \sin\left(\frac{\pi T}{T_0}\right)}{(2\alpha)^3 B_C}\right]^{\frac{T_0}{T}}$$

where σ_0 is a conductivity prefactor and T_0 is a characteristic parameter describing the width of the exponential DOS. The elementary charge is indicated by e, and B_C is a critical number for the onset of percolation and given by 2.8 for 3D systems. The Vissenberg-Matters model predicts an increase of the field-effect mobility with increasing charge carrier density, as the accumulated charges fill the lower-lying states of the organic semiconductor first and any additional charges in the accumulation layer will occupy states at relatively high energies. Thus, additional charges will require a lower thermal energy to hop between sites [71]. Equation 1.2 is valid for temperatures well below T_0. The model was successfully used to describe the

temperature and density dependent transport in unipolar and ambipolar transistors [72].

An alternative theory worth mentioning for understanding the effects of disorder is the multiple-trapping-and-release (MTR) mechanism, which was successfully used to explain the transport in amorphous Si and metal oxide semiconductors [73, 74]. The MTR model assumes that the transport takes place in extended, delocalized states above a so-called mobility edge, and that carriers in levels below are effectively trapped in localized states. Most carriers are trapped, and charge transport takes place by a small fraction of carriers that are thermally activated into the delocalized states above the mobility edge. The MTR approach results in a similar carrier density and temperature dependence as variable range hopping, which makes it difficult to distinguish between the models. The MTR model has, however, been claimed to be more appropriate for describing the charge transport in microcrystalline polymers, such as polythiophene derivatives [74, 75].

Tanase and coworkers proposed a unification of the mobility in field-effect transistors and diodes by empirically combining the diode and field-effect mobilities:

$$\mu_{unified}(p,T) = \mu(0,T) + \mu_{VM} \tag{1.3}$$

where μ_{VM} is the Vissenberg-Matters mobility, expressed above as Eq. 1.2, and $\mu(0,T)$ is the temperature-dependent hole mobility at low field and low carrier density, found from diode measurements:

$$\mu(0,T) = \mu_{\infty} \exp\left(-\frac{\Delta}{k_B T}\right)$$

with a mobility prefactor μ_{∞} and an activation energy Δ. This unified mobility was used to explain the enhanced currents found in polymer based diodes [68, 76].

Pasveer and coworkers established a unified theoretical description of the full temperature, density, and field dependence of the carrier mobility. Their model is based on Gaussian disorder and takes into account the fact that only one carrier can occupy a site, due to the high Coulomb penalty for the presence of two or more carriers. At room temperature the carrier density dependence is dominant, only for low temperatures and high electric fields the field dependence becomes important. In the limit of low carrier densities, carriers can be considered independent of each other and, as a result, their mobility is nearly constant. Above a certain concentration there is a crossover to a transport regime in which the mobility increases with increasing carrier concentration. The parametrization resulting from the Pasveer approach is optimized for low carrier densities. Therefore, the model is not suitable for describing the transport in transistors, where charge densities are high. Several other transport models were developed, all yielding a crossover from a density-independent mobility regime to a density dependent regime [77].

The mobility in field-effect transistors is typically orders of magnitude higher than in diodes, as will be addressed in Chapter 4 and the electric field is low. Therefore, for organic field-effect transistors the second term in Eq. 1.3 dominates the mobility, and the first term can be neglected. The mobility model developed

by Vissenberg and Matters, Eq. 1.2, is therefore sufficient to describe the mobility in organic field-effect transistors, and will be used throughout this thesis.

1.4 Organic transistors

The basic building block for organic electronics is the organic field-effect transistor (OFET). In this section the working principles of OFETs will be discussed, their current voltage characteristics, and how to extract information from them.

Organic field-effect transistors

An OFET consists of a thin semiconductor layer, a gate dielectric, and three electrodes, as illustrated in Fig. 1.1a. The source and drain electrodes are connected to the semiconductor, whereas the gate electrode is electrically isolated from the semiconductor by the gate dielectric. Normally, voltage is applied to the gate electrode (V_G) and drain electrode (V_D) with respect to the source electrode, which is grounded ($V_S = 0$ V). The current between the source and drain electrodes (I_D) depends on both the gate bias and drain bias, and different operating regimes can be identified.

In this thesis, organic transistors are discussed which operate in unipolar p-type accumulation mode. The current in these transistors is carried by holes, i.e. positive charge carriers. **Fig. 1.5a** shows a typical transfer curve, the drain current as a function of gate bias at constant drain bias, of a p-type transistor. When a negative gate bias is applied, holes accumulate at the semiconductor-dielectric interface. The accumulated holes form a conducting path between the source and drain electrodes, allowing a current to flow. On the other hand, when a positive gate bias is applied, the semiconductor is depleted of holes, and the transistor is switched off. The transition from the on to the off state is clearly visible in the transfer curve. The gate bias at which the transistor switches between the low current

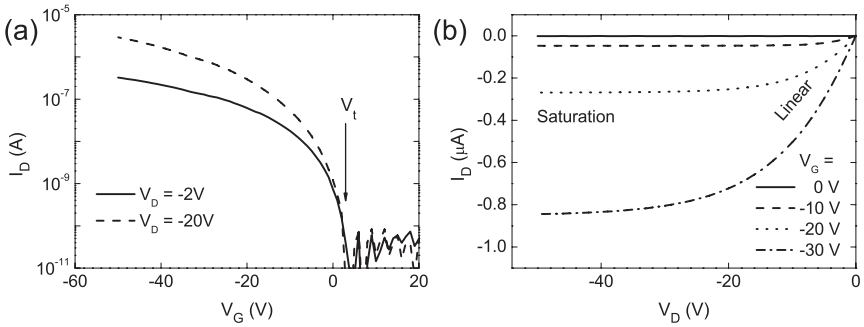

Figure 1.5. Typical current-voltage characteristics of a p-type organic field-effect transistor. (a) transfer characteristics, indicating the abrupt switching at the threshold voltage, V_t, from the off-state to the on-state. (b) Output characteristics demonstrating the linear and saturation regimes. The semiconductor was MDMO-PPV, the width and length were 2500 µm and 10 µm, and the measurement temperature was 330 K.

depletion regime and the high current accumulation regime is the threshold voltage, V_t [78]. The threshold voltage is mainly determined by (un)intentional doping of the semiconductor film, and dipoles and charged states at the semiconductor-dielectric interface [79–81]. Figure 1.5b shows the output characteristics, the drain current as a function of drain bias at fixed gate bias, of the same transistor. When the drain bias is much smaller than the gate bias, the current depends linearly on both gate bias and drain bias. The current saturates when the drain bias is larger than the gate bias. The linear and saturation regimes are indicated in Fig. 1.5b.

The current in both the linear and saturation regimes is often analyzed using classical analytically MOS equations. These equations are derived using the so called gradual channel approximation, which assumes that the field perpendicular to the current, induced by the gate bias, is much larger than the electric field between source and drain [71]. The mobility is assumed to be independent of the carrier density. Furthermore, contact resistance, doping density and short channel effects are neglected. The resulting gradual channel expression for the current in accumulation is given as:

$$I_D = \frac{WC_i}{L}\mu\left[(V_G - V_t)V_D - \frac{1}{2}{V_D}^2\right] \tag{1.4}$$

where W and L are the width and length of the transistor channel, C_i is the gate capacitance per unit area, and μ is the carrier mobility. When no source-drain bias is applied, the charge carrier concentration in the transistor channel is uniform between the source and drain. In the linear regime, i.e. $|V_D| \ll |V_G - V_t|$, the concentration is still rather uniform, with a linear gradient from the carrier injecting source to the extracting drain. For the linear regime, Eq. 1.4 can be simplified to:

$${I_D}^{lin} = \frac{WC_i}{L}\mu_{lin}(V_G - V_t)V_D \tag{1.5}$$

The usual way to extract the linear mobility, μ_{lin}, from the measurement is now to take the derivative of the current to the gate bias, and reorganize Eq. 1.5 to get:

$$\mu_{lin} = \frac{L}{WC_iV_D}\frac{\partial {I_D}^{lin}}{\partial V_G} \tag{1.6}$$

When the drain voltage is further increased, a point $V_D = V_G - V_t$ is reached. The difference between the gate bias and the local channel potential near the drain is then below the threshold voltage. Consequently, a depletion region forms near the drain, and the channel is 'pinched off'. Further increasing the drain voltage will not substantially increase the current but leads to an expansion of the depletion region. The current in this saturation regime, i.e. $|V_D| \gg |V_G - V_t|$, can be derived from Eq. 1.4 by substituting $V_D = V_G - V_t$, yielding:

$${I_D}^{sat} = \frac{WC_i}{2L}\mu_{sat}(V_G - V_t)^2 \tag{1.7}$$

The saturation mobility, μ_{sat}, can be extracted from the measurement by rearranging Eq. 1.7, resulting in:

$$\mu_{sat} = \frac{L}{WC_i} \frac{1}{(V_G - V_t)} \frac{\partial {I_D}^{sat}}{\partial V_G} \tag{1.8}$$

We note that the linear or saturated mobilities extracted in this way are device parameters, and do not necessarily reflect the 'true' mobility of the semiconductor. The extracted value can for example depend on the carrier density or gate bias, the permittivity of the gate dielectric, the transistor geometry and architecture, or contact resistance [82]. An analytical model which accounts for the gate bias dependence was developed previously. This model is based on the carrier density dependent Vissenberg-Matters conductivity and will be introduced in detail in Chapter 3.

Dual-gate transistors

Control of the threshold voltage is essential for any envisioned application of OFETs. For logic gates, the threshold voltage determines the trip point, which is the input bias at which the gate switches the output signal. In sensing applications, the threshold voltage signifies the bias at which the largest change in current occurs, i.e. the point of the highest sensitivity. The threshold voltage of an OFET is typically slightly positive, yielding normally-ON devices. Therefore, integrated circuits are based on inverters with a so-called zero-V_{GS}-load topology, whereby the gate of the load transistor is connected to its source. This topology suffers from an inherently small noise margin, which is a measure for the maximum allowed spurious signal that can be accepted by the gate while still giving the correct operation.

For standard Si transistors, the threshold voltage can be accurately set by the amount of doping applied by ion implantation. Local doping of individual OFETs in a circuit is not an option, and therefore a different approach is desirable to externally set the threshold voltage. Several options have been reported, such as modification of the dielectric to set the interface charge or the use of a gate metal with a specific work function [83].

A dual-gate transistor is an alternative solution to set V_t. As compared to a conventional thin-film transistor, the layout of a dual-gate transistor contains an additional gate dielectric and electrode, as schematically depicted in **Fig. 1.6a**. A bias to the second gate electrode modifies the charge carrier distribution in the channel accumulated by the first gate. Effectively, the second gate can accurately set V_t, which can be used, for example, to improve the noise-margin of logic gates dramatically [84].

One of the first dual-gate transistors was based on CdSe as the semiconductor, and reported in 1981 for use in flat panel displays [85]. The first organic dual-gate transistors were reported in 2005 by several groups [86–90]. Advantages reported in almost all papers are a steeper subthreshold slope and an increased gate modulation, with a higher on-current and lower off-current. However, the main advantage

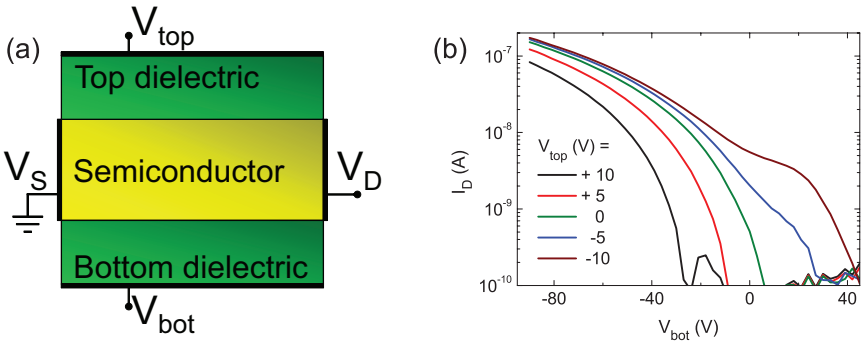

Figure 1.6. (a) Schematic representation of a dual-gate organic field-effect transistor. (b) Typical transfer characteristics of a *p*-type dual-gate OFET. Bottom-sweeps are shown for fixed top gate bias.

is that the threshold voltage can be set as a function of the applied second gate bias.

Tuning of V_t by using a second gate has been applied to make logic gates and integrated circuits more robust. Using dual-gate technology, complex circuits such as a processor and a Braille sheet display were demonstrated. Also, a dual-gate transistor itself can be configured to act as a self-contained logic gate, such as an AND gate. Another promising application is in biosensing, where a dual-gate can be used as an ion-sensitive field-effect transistor. By using a double-gate structure, the sensitivity of the sensor can be enhanced, because the transistor acts as a build-in amplifier [83].

Typical transfer characteristics of a *p*-type dual-gate transistor are shown in Fig. 1.6b. The drain current is presented as a function of the bottom gate bias, for fixed top gate bias. It is clear that the threshold voltage shifts as a function of the top gate bias. The origin of the shift can be understood from the capacitive coupling of both gates. Both gates can accumulate or deplete charges in the semiconductor. Accumulated charges are concentrated in a few nanometers at the dielectric interface. If the semiconductor is sufficiently thick, two spatially separated channels can form. When the top gate is grounded, no charge is accumulated or depleted. Hence, the influence of the top gate is negligible, and the transistor operates as a conventional single-gate transistor.

For positive top gate bias, holes are depleted from the semiconductor. There are no electrons to screen the top gate bias, so its influence reaches to the bottom channel. At the bottom interface, mobile charges are accumulated by the bottom gate bias, but depleted by the top gate. To come to be the original current, the top gate has to be compensated for and, therefore, the bottom gate bias has to be increased. Effectively, the transfer curve is shifted to the left in Fig. 1.6b. For negative top gate bias, holes are accumulated at the top gate interface. A conducting channel is formed, increasing the total drain current. The top channel is only depleted by the bottom gate at positive bias. Effectively, the entire transfer curve is shifted to the right.

The shift in threshold voltage can be quantified from the total induced charge by the two gates, and depends on the ratio of the capacitances of the two gate dielectrics. If the top gate is fixed and the bottom gate is swept, the shift in the threshold voltage from the perspective of the bottom gate is given by [88, 91, 92]:

$$\Delta V_{t,bot} = -\frac{C_{top}}{C_{bot}} \Delta V_{top} \tag{1.9}$$

where C_{top} and C_{bot} are the capacitances per unit area of the top and bottom dielectric, and V_{top} is the top gate bias. Hence the second gate can set V_t, but at the cost of an extra electrical contact with its accompanying additional processing steps during fabrication.

The charge transport in dual-gate transistors is not yet fully understood. The transfer curves often show a typical 'shoulder', meaning that in depletion the transconductance does not monotonically decrease with increasing gate bias. This anomaly is illustrated in Fig. 1.6b and has been ascribed to the capacitance of the semiconductor [91]. The depleted part of the semiconductor forms a capacitor in series with the gate dielectric. When the semiconductor capacitance is comparable to the gate capacitance, it should not be ignored. Then, in Eq. 1.9, C_{top} and C_{bot} have to be replace by:

$$C_{eff} = \frac{C_{gate} C_{sc}}{C_{gate} + C_{sc}} \tag{1.10}$$

for the channel that is in depletion, where C_{gate} is the associated gate capacitance and C_{sc} is the semiconductor capacitance. However, also in dual-gate transistors with a semiconductor with a much higher capacitance than the bottom and top capacitances, a shoulder can be observed. Therefore Eq. 1.10 is not sufficient to explain the anomaly. A shoulder could, for example, also arise from a non-uniform DOS. The charge transport and the origin of the shoulder are investigated in Chapter 7 by deliberately varying the semiconductor thickness.

Ferroelectric transistors as memory

In many of applications of organic electronics there is a need to store information, preferably using a non-volatile memory that is rewritable and can be read-out electrically in a non-destructive way. For example, RFID tags need to be able to send and receive stored information by means of a radio signal. An RFID tag derives power only when it is in range of the radio signal, which means that the circuit does not have a power source constantly available. A volatile memory technology, which needs regular refresh operations to prevent data loss, is therefore not suitable. A non-volatile memory, a mechanism where the information is preserved after removing the power source, is the memory of choice. Furthermore, easy electrical and non-destructive read-out and rewritability are desired properties to obtain a more universally applicable memory.

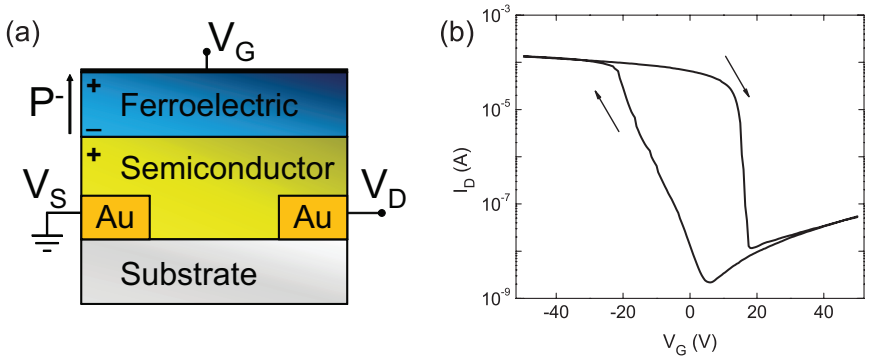

Figure 1.7. (a) Schematic representation of an organic ferroelectric field-effect transistor (FeFET). (b) Typical transfer curve of a *p*-type FeFET, where the arrows indicate the scan direction.

Ferroelectric field-effect transistors (FeFETs) are attractive for this purpose due to fast non-destructive data read-out and low power consumption [51, 93]. A ferroelectric material exhibits a bistable, remnant electric polarization, P_R, that can be switched by electric fields exceeding a certain critical field, the coercive field, E_C. In a FeFET, the gate dielectric is replaced by a ferroelectric material, as illustrated in **Fig. 1.7a**. Because of its remnant polarization, the ferroelectric layer can adopt either of two stable polarization states, which persist when no biases are applied. A typical transfer curve of a unipolar *p*-type FeFET is presented in Fig. 1.7b. Switching from one polarization state to the other occurs by applying a gate bias exceeding the coercive field. Depending on the orientation of the polarization, positive or negative charges can be induced in the semiconductor at the semiconductor-ferroelectric interface. The induced surface charge density shifts the onset of channel accumulation towards either more negative or positive gate bias. Hence, a gate bias window, defined mainly by the coercive field, exists wherein the drain current may have either of two levels depending on the actual polarization state of the ferroelectric gate dielectric. The corresponding high and low drain current levels can be used to define Boolean '0' and '1' states of a non-volatile

memory with non-destructive read-out [51].

The first functional organic FeFETs were demonstrated in 2004 and 2005 [94, 95]. The most commonly used organic ferroelectric material in FeFETs is the random copolymer poly(vinylidenefluoride-co-trifluorethylene) (P(VDF-TrFE)). Since their introduction, many FeFETs using different organic and metal oxide semiconductors have been reported [96–101].

Details of the device physics however remain elusive. A question is for instance, what is the contribution of the linear and the ferroelectric polarization to the drain current? And is the polarization stable in the off-state? To answer these questions a quantitative analysis is presented in Chapter 9, which until now has not been reported for organic FeFETs.

1.5 Outline of this thesis

Central in this thesis is the impact of the charge-carrier-density dependent mobility of disordered organic materials on the charge transport in organic transistors. Charge transport calculations are used as a tool to get a thorough understanding of the transport behavior in several recently developed organic transistor designs.

In **Chapter 2**, a detailed overview is presented of the materials, transistor fabrication methods and measurement techniques used throughout this thesis. Likewise, the numerical calculation methods and analytical approaches are presented in **Chapter 3**.

In **Chapter 4**, the hole mobility in a doped and undoped polymer semiconductor is experimentally probed over a wide carrier density range. Combining the experimental mobility from doped and undoped diodes and transistors at different carrier density ranges, establishes a smooth relation of the mobility versus density over the whole carrier density range.

In the Chapter 4, we use ohmic contacts for holes, so contact resistance or charge injection barriers can be neglected. However, larger barriers might lead to a severe underestimation of the extracted mobility. Therefore, we address the question under which circumstances the injection barrier does play a role in **Chapter 5**. The charge injection barriers in organic field-effect transistors (OFETs) seem to be far less critical as compared to organic light-emitting diodes (OLEDs). We show that the origin is image-force lowering of the barrier due to the gate bias at the source contact. The gate bias indirectly narrows the depletion region at the injecting contact, thereby increasing the carrier injection. The interpretation is supported by 2D numerical transport simulations. Injection barriers up to 1 eV can be surmounted.

The injection barrier for electrons in *p*-type OFETs is larger than 1 eV, for which Chapter 5 predicts severe limiting of the carrier injection. Experimentally, an inversion current in *p*-type OFETs is not observed, which can be due to trapping of electrons or to negligible electron injection. In **Chapter 6**, we distinguish between both cases by studying the depletion current of *p*-type transistors based on a deliberately doped organic semiconductor. We show unambiguously that no inversion layer is formed. Numerical calculations show that for electron injection

barriers > 1 eV thermodynamically equilibrium is not reached within the time frame of the experiment.

Chapters 7–9 focus on the device physics of three specific organic transistor configurations: Dual-gate OFETs, organic monolayer FETs, and organic ferroelectric FETs.

In **Chapter 7**, the charge carrier distribution in dual-gate field-effect transistors is investigated as a function of semiconductor thickness, supported by 2D numerical simulations. For semiconductor thicknesses larger than the accumulation width, two spatially separated channels are formed. The two channels in combination with a carrier density dependent mobility cause a typical shoulder in the transfer characteristics. In contrast, a semiconducting monolayer transistor has only a single channel. The charge carrier density, and consequently the mobility, are virtually constant in the monolayer. The current changes monotonically with applied gate biases, leading to transfer curves without a shoulder.

The thickness of the accumulation channel in an OFET is several nanometers, and the carrier density decreases with distance from the dielectric interface. However, the accumulated charge in a monolayer transistor is physically confined to the monolayer, which is only about 2 nm thick. In **Chapter 8** we found a signature of charge confinement by comparing the temperature dependence of monolayer transistors and conventional OFETs.

In **Chapter 9**, an analytical model is presented that describes the charge transport in organic FeFETs. The model combines an empirical expression for the ferroelectric polarization with the density dependent mobility in organic semiconductors. Transfer curves can be calculated with parameters that are directly linked to the physical properties of both the comprising ferroelectric and semiconductor materials. The model describes both unipolar FeFETs and ambipolar FeFETs, which supports both holes and electrons. The description can be used to analyze FeFET data consistently and can be easily adapted for use in circuit simulators.

1.6 Abbreviations used in this thesis

1D, 2D, 3D	one, two, three-dimensional
ID	drain current
2DEG	two-dimensional electron gas
α^{-1}	effective overlap parameter
AFM	atomic force microscopy
B_C	critical number for the onset of percolation
C_i	gate capacitance per unit area
C_{top} (C_{bot})	capacitance per unit area of the top (bottom) dielectric
C–V	capacitance-voltage measurement
CMOS	complementary metal-oxide-semiconductor
d_{sc}	semiconductor thickness
DOS	density of states
$\Delta\epsilon = \epsilon_j - \epsilon_i$	energetic difference between hopping sites
$\Delta\varphi$	barrier lowering
e	elementary charge
ε	dielectric constant
E_g	bandgap
E_C	coercive field
φ_B	effective injection barrier
φ_{B0}	energy difference between metal workfunction and HOMO
φ_p (φ_n)	quasi Fermi level for holes (electrons)
FeFET	ferroelectric field-effect transistor
FET	field-effect transistor
HOMO	highest occupied molecular orbital
IC	integrated circuit
ITO	indium tin oxide
J_p (J_n)	hole (electron) current density
k_B	Boltzmann constant
L	transistor channel length
LUMO	lowest unoccupied molecular orbital
MDMO-PPV	poly(2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylene vinylene)
MEH-PPV	poly(2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene)
MEK	methyl ethyl keton
MTR	multiple-trapping-and-release
MOS	metal-oxide-semiconductor
μ	charge carrier mobility
μ_p (μ_n)	hole (electron) mobility
N_D (N_A)	ionized donor (acceptor) densities
n_i	intrinsic carrier density
N_V (N_C)	effective DOS of valence (conduction) band
OFET	organic field-effect transistor
OLED	organic light-emitting diode

p (n)	hole (electron) density
p_c (n_c)	contact hole (electron) density
P	ferroelectric polarization
P_R	remnant polarization
P_S	saturated polarization
P3HT	poly(3-hexylthiophene)
PCBM	(6,6)-phenyl-C_{61}-butyric acid methyl ester
PEDOT:PSS	poly(3,4-ethylenedioxythiophene):poly(styrenesulfonic acid)
PIBMA	poly(isobutyl methacrylate)
PMMA	poly(methyl methacrylate)
PPV	poly(p-phenylene vinylene)
PTV	poly(2,5-thienylene vinylene)
P(VDF-TrFE)	poly(vinylidenefluoride-co-trifluorethylene)
ψ	electrostatic potential
Q_{if}	interface charge density
R	recombination rate
R_{ij}	spatial distance between hopping sites
RFID	radio frequency identification
SAMFET	self-assembled monolayer field-effect transistors
σ_0	conductivity prefactor
SCLC	space-charge-limited current
T	temperature
T_0	parameter describing the DOS width
T5-silane	chloro-ethyl-quinquethienyl undecyl dimethylsilane
T6	α-sexithiophene
TCFOS	trichloro(1H,1H,2H,2H-perfluorooctyl)silane
TIPS-PEN	triisopropyl-silylethynyl pentacene
υ_0	attempt-to-jump frequency
V_D	drain bias
V_G	gate bias
V_S	source bias
V_{pinch}	pinch-off voltage
V_{SO}	switch-on voltage, gate bias at onset of accumulation
V_t	threshold voltage
V_{top} (V_{bot})	top (bottom) gate bias
$V_{t,top}$ ($V_{t,bot}$)	top (bottom) gate threshold voltage
V_x	potential difference between gate bias and local channel potential at x
V-M	Vissenberg and Matters
W_{ij}	charge carrier hopping rate
W	transistor channel width
x (y)	direction along (perpendicular) semiconductor-dielectric

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Materials and experimental methods

2

A wide range of materials and processing methods is available to fabricate organic transistors. In this chapter, the materials and processing methods used to prepare the devices in this thesis will be described, as well as the methods to characterize them. The fabrication of an organic transistor consists of several processing steps. The majority of the transistors in this thesis are made using standardized test substrates. The substrates are prefabricated with a gate dielectric, and source and drain electrodes, whereas the substrate itself acts as the gate electrode. Semiconductors were applied on the substrates by spin-coating, self-assembly and vapor deposition. In the case of dual-gate transistors and ferroelectric transistors, a second insulating layer was deposited by spin-coating, followed by evaporation of a metal top gate.

2.1 Substrates and materials

The test substrates were fabricated on heavily n-doped 150 mm Si wafers that act as a common gate. A 200 nm thermally grown SiO_2 layer passivated with hexamethyldisilazane was used as gate dielectric. The gate capacitance depends on the thickness of the dielectric and its dielectric constant, which is 3.9 for SiO_2. Au source and drain electrodes with a thickness of 100 nm were lithographically defined, using a 10 nm Ti adhesion layer. A wafer contains several dozen substrates, and on each substrate a large number of transistor structures is defined, as depicted in **Fig. 2.1**. The large number of identical substrates on a single wafer provides a high degree of experimental reproducibility. An actual transistor pattern is shown in Fig. 2.1c. Several series of these patterns are available on a substrate, with systematically varying channel width and length.

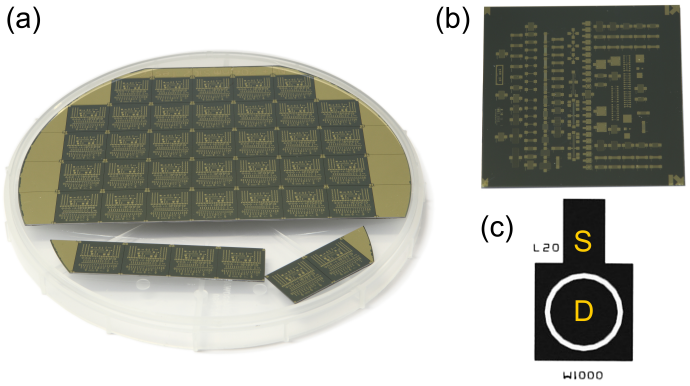

Figure 2.1. (a) A photograph of a 150 mm wafer containing several test substrates. (b) Photograph of a test substrate with various Au transistor structures. (c) Optical micrograph of a transistor test structure with a channel length and width of 20 µm and 1000 µm. The source and drain electrodes are indicated.

The chemical structures of the organic semiconductors and insulators used throughout this thesis are shown in **Fig. 2.2**. As polymer semiconductors, a polythiophene derivative and phenylene-vinylene derivatives were used to allow for comparison with literature. To fabricate transistors with an extremely thin semiconductor, a self-assembling molecule and the small molecule alpha-sexithiophene were chosen. All transistors were fabricated in a N_2 atmosphere in a glovebox. A typical value for the dielectric constant of organic semiconductors is 3, which is used in all the calculations.

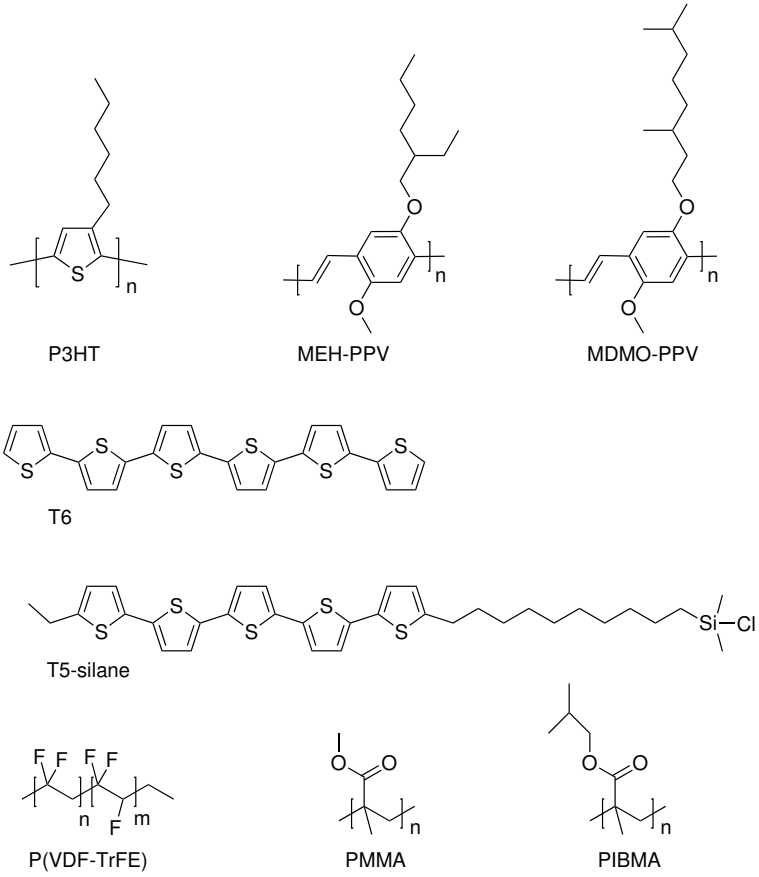

Figure 2.2. Chemical structures of the materials used in this thesis.

2.2 Sample fabrication and measurements

Regio-regular poly(3-hexylthiophene) (P3HT) was obtained from Imperial College London and used without further purification. The molecular weight was 33 000 g/mol as measured by GPC and the regio-regularity was > 97%, as measured by NMR. Alternatively, P3HT was purchased from Rieke Metals, Inc. and purified before use, by dissolving in distilled toluene, dedoped with hydrazine and precipitated in methanol. The fraction collected was Soxhlet extracted with methanol, n-hexane and dichloromethane until the extraction solvent was colorless. The dichloromethane fraction was precipitated in methanol, collected, dissolved in chloroform and precipitated again in methanol. The collected fraction was dried under vacuum and stored under a N_2 atmosphere. To deposit a film of P3HT, the polymer was spin-coated from chloroform, with a concentration of typically 20 mg/ml. The resulting film thickness was between 30 nm and 200 nm, depending on the concentration and spin-coating speed. Subsequently, the transistors were annealed in a vacuum oven at 150 °C for 2 hours, to remove any remaining solvent.

Two poly(phenylene-vinylene) (PPV) derivatives were used in this thesis. The first was poly(2-methoxy-5-(3',7'-dimethyloctyloxy)-1,4-phenylene vinylene) (MDMO-PPV). To form a film, MDMO-PPV was spin-coated from chlorobenzene and the transistors were subsequently annealed at 100 °C in vacuum. The other PPV derivative was poly(2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene) (MEH-PPV), spin-coated from toluene with a concentration of 5 mg/ml.

Transistors with a semiconducting monolayer were fabricated using self-assembly and by thermal evaporation. Self-assembled monolayer field-effect transistors (SAM-FETs) of chloro(11-(5""-ethyl-2,2:5',2" :5",2"':5"',2""-quinquethien-5-yl)undecyl) dimethylsilane (T5-silane) were self-assembled from a toluene solution, as reported previously [1, 2]. Alternatively, a monolayer of α-sexithiophene (T6, Sigma Aldrich) was evaporated at a rate of about 0.6 nm/min onto a substrate that was held at elevated temperature (120 °C).

The evaporation time of T6 molecules was systematically increased to study the layer growth. Atomic force microscopy (AFM) clearly shows height steps of approximately the molecular length of T6 (∼2.4 nm), as shown in **Fig. 2.3**. The first monolayer is fully closed. Large islands of the second layer, and smaller islands of the next layers, start to form, but are not percolating. Therefore, only the first monolayer contributes to the charge transport, and the sample can be considered a monolayer transistor.

In Chapter 4, also diode structures were used in addition to transistors. Hole-only diodes were fabricated on glass slides with a patterned layer of indium tin oxide (ITO). A 60 nm thin layer of poly(3,4-ethylenedioxythiophene) doped with poly(styrenesulfonic acid) (PEDOT:PSS) was spin-coated on top of the ITO as ohmic anode. The mobile ions in PEDOT:PSS however hamper reliable capacitance-voltage (C–V) measurements. Hence Schottky diodes were fabricated with a Au anode for C–V measurements. After spin-coating P3HT, all diodes were annealed at 150 °C for 2 hours in vacuum. Hole-only diodes were finished by evaporating an electron blocking contact of 20 nm Pd and 80 nm Au. Schottky diodes were finished by evaporating a cathode of 90 nm Al.

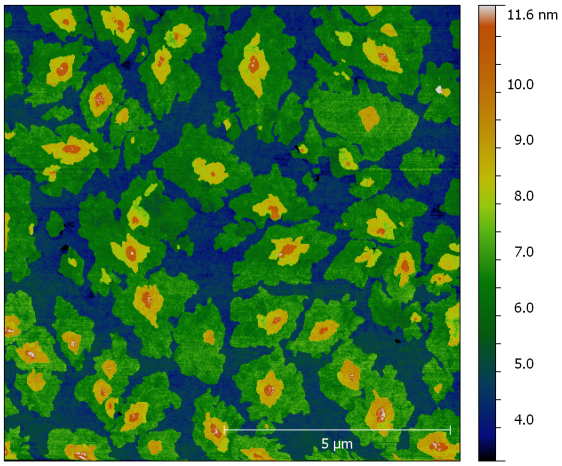

Figure 2.3. Atomic force microscopy image of evaporated T6 in the transistor channel. The first monolayer is fully closed and islands of the next layers start to grow.

Dual-gate transistors were fabricated starting with a standard substrate. Dual-gate transistors with a 'conventional' thin-film semiconductor were prepared by spin-coating a film of MEH-PPV. For dual-gate transistors with an extremely thin semiconductor, a semiconducting self-assembled monolayer was used. Subsequently, poly(methyl methacrylate) (PMMA, Sigma-Aldrich) or poly(isobutyl methacrylate) (PIBMA, Sigma-Aldrich) were applied as second gate dielectric. PMMA was spin-coated from butanone (50 mg/ml) and PIBMA from butanol (8% w/w), resulting in a layer thickness of 300 nm and 600 nm, respectively. Although their molecular structure is very similar, PMMA has a dielectric constant of 3.6, and that of PIBMA is 2.2. The devices were finished by evaporation of a Ag or Au top gate electrode.

For the ferroelectric transistors and capacitors, the ferroelectric random copolymer poly(vinylidenefluoride-co-trifluoroethylene) (65%–35%) (P(VDF-TrFE)) was used. The P(VDF-TrFE) was purchased from Solvay, Belgium and was used as received. Ferroelectric capacitors were fabricated on glass slides with Ag bottom electrodes. A layer of P(VDF-TrFE) was spin-coated onto the substrates from a methyl ethyl keton solution (MEK) with a concentration of 30–50mg/ml. Prior to spin-coating the solution was filtered using a 1 µm PTFE filter. The film thickness was 300–400 nm. The films were subsequently annealed at 140 °C in a vacuum oven (10^{-1} mbar) to enhance the crystallinity of P(VDF-TrFE). A top contact of Ag was evaporated through a shadow mask to finish the capacitors, with a device area of $1 \times 1\text{mm}^2$. Unipolar ferroelectric transistors were fabricated on standard substrates. Measurements were done on transistors with a channel length varying from 5 µm to 40 µm while the channel width was kept constant at 10 000 µm. A film of P3HT was spin-coated from chloroform and subsequently a P(VDF-TrFE) layer was spin-coated from MEK. We note that MEK is an orthogonal solvent for P3HT. The film thicknesses were 30 nm for P3HT and 300–400 nm for P(VDF-

TrFE). The stack was annealed in a vacuum oven at 140 °C. To form the staggered top gate of the FeFETs, a 70 nm Ag layer was evaporated through a shadow mask.

All electrical characterization of the transistors was performed the dark and in vacuum ($< 10^{-4}$ mbar). A measurement setup is shown in **Fig. 2.4**. Current–voltage measurements were performed using a Keithley 4200 Semiconductor Measurement System (at the University of Groningen) or an Agilent 4155C Semiconductor Parameter Analyzer (Philips Research, Eindhoven). Film thicknesses were measured with a Dektak 6M profilometer. Ferroelectric capacitors were characterized using a home-built Sawyer-Tower circuit at a frequency of 100 Hz. In such as circuit, the polarization of the ferroelectric layer can be measured by measuring the voltage over a large reference capacitor connected in series with the sample. Current–voltage characteristics of diodes were recorded in the dark and in nitrogen atmosphere using a Keithley 2400 SourceMeter. Capacitance–voltage measurements of Schottky diodes were conducted with a Solartron SI 1260 impedance/gain-phase analyzer.

In Chapters 4 and 6 we make use of a doped semiconductor. Transistors and Schottky diodes were doped by exposure to a vapor of trichloro(1H,1H,2H,2H-perfluorooctyl)silane (TCFOS, Sigma Aldrich). The measurement chamber was evacuated to less than 10^{-4} mbar. Then, 20–60 µl TCFOS was injected into an antechamber. A valve to the measurement chamber was opened resulting in a TCFOS partial pressure of 10^{-2} mbar. The transfer characteristics of the transistors were measured as a function of exposure time [3]. We note that in the case of Schottky diodes the evaporation of the top electrode was performed after the doping process to guarantee a uniformly doped semiconductor.

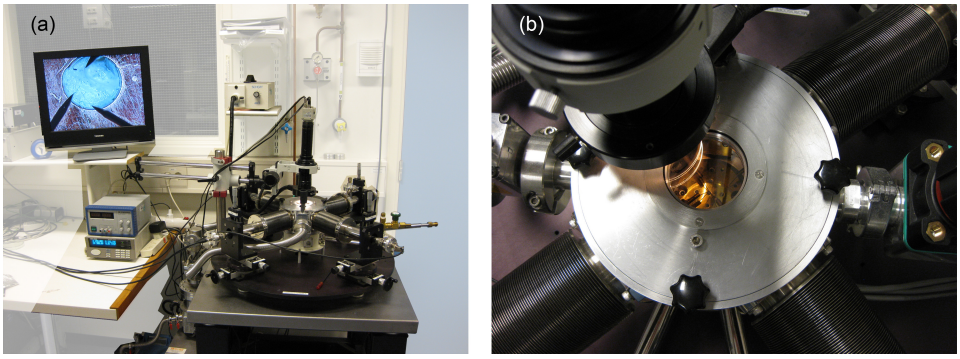

Figure 2.4. (a) Photograph of the transistor measurement setup, showing on the right a probe station, and on the left a monitor and the temperature- and vacuum controls. The position of the probes can be tracked with the camera-monitor system. The irrelevant part of the image was blurred. (b) Close-up of the vacuum container with the sample stage.

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Computational methods

3

In an organic field-effect transistor, the charge carrier density in the semiconductor is controlled by the gate electrode. The charge carrier distribution in the semiconductor upon accumulation is not constant. The density is high at the semiconductor-dielectric interface, but decreases with the distance squared. The current between the source and drain electrodes depends on the charge carrier density and the corresponding mobility. At each point in the semiconductor the applied gate bias determines the local carrier density and the resulting local mobility. The three-dimensional (3D) distribution of density and mobility prevents a straightforward calculation of the source–drain current. However, the geometry of the transistor is such that approximations can be made to simplify calculations of the charge transport. The geometry of a bottom-gate bottom-contact transistor is depicted in **Fig. 3.1**. The transistor width, W, is much larger than the length, L. Hence, charge transport along the width can be assumed to be uniform, allowing for 2D simulations. To arrive at an analytical solution, additional approximations are needed. Typically the gradual channel approximation is used, where the electric field perpendicular to the film is assumed to be much larger than in the source drain direction. In this way the transport can effectively be treated as a 1D problem. To avoid excess approximations and to verify the analytical solutions 2D numerical simulations are indicated. In this Chapter, the numerical and analytical methods used throughout this thesis are introduced.

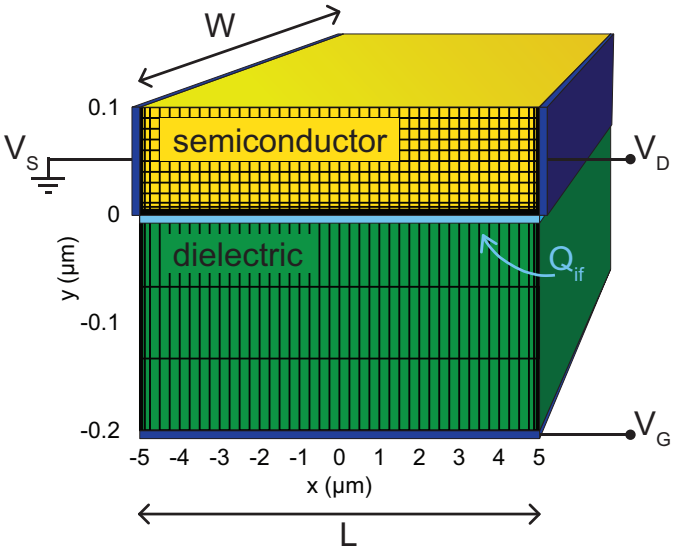

Figure 3.1. Schematic representation of a bottom-gate bottom-contact transistor and an example of the rectangular grid used in the numerical charge transport calculations. Close to the contacts and the semiconductor-dielectric interfaces the grid size decreases exponentially. The semiconductor thickness and dielectric thickness are 100 nm and 200 nm, the channel length, L, is 10 µm. The transport along the width, W, is assumed to be uniform. Interface charge, Q_{if}, is defined at the semiconductor-dielectric interface.

3.1 Numerical transport calculations

The electrical transport is governed by Poissons equation, the continuity equations and the drift-diffusion equations [1, 2]. Poissons equation relates the local potential to the charge density:

$$-\varepsilon_0 \varepsilon_{sc} \nabla^2 \psi = e(p - n + N_D - N_A) \tag{3.1}$$

where ψ is the electrostatic potential, and p and n are the hole and electron densities. N_D and N_A are the ionized donor and acceptor densities, ε_0 is the vacuum permittivity, ε_{sc} is the relative permittivity of the semiconductor and e is the elementary charge. The electron and hole density can vary with time due to recombination or due to a gradient in the current. The changes are expressed in the continuity equations as:

$$e\frac{\partial p}{\partial t} = -\nabla J_p - eR \tag{3.2a}$$

$$e\frac{\partial n}{\partial t} = \nabla J_n - eR \tag{3.2b}$$

where J_p and J_n are the local hole and electron current density and R the Langevin recombination rate [3]. The current densities depend on the local electric field and gradients in the density of holes and electrons. The corresponding drift-diffusion currents for holes and electrons then follow from:

$$J_p = e\mu_p\left(pE - \frac{k_B T}{e}\nabla p\right) \tag{3.3a}$$

$$J_n = e\mu_n\left(nE + \frac{k_B T}{e}\nabla n\right) \tag{3.3b}$$

where μ_p and μ_n are the hole and electron mobilities, k_B is the Boltzmann constant, T is the temperature and E is the electric field. The electric field is the gradient of the electrostatic potential, implying that Eqs. 3.1–3.3 are coupled. They are solved self-consistently yielding locally p, n and ψ. To find the current in a transistor, coupled to the solution for p, n and ψ, the device has to be divided in discrete points. A steady-state solution was found iteratively, using the Newton method [1, 2]. An expression for the mobility is required and boundary conditions for the contacts have to be imposed.

Software packages to numerically calculate electrical transport in microelectronic devices are commercially available. Most packages are designed for conventional crystalline semiconductors, i.e. the underlying physics is based on band transport. For accurate simulations of organic semiconductors, a software package is required where a charge carrier dependent mobility, any injection model and bulk doping can easily be implemented [4–8]. Here we used the CURRY package, previously developed at Philips Research, because it offers the required flexibility to implement user-defined functions [1, 9–11].

A 2D rectangular mesh was used to map the device structure to be simulated. A typical example of a bottom-gate bottom-contact transistor is presented in Fig. 3.1. Perpendicular to the gate, the mesh spacing in the semiconductor was several nm. To accurately calculate the large gradient in carrier density close to the semiconductor-dielectric interface, the spacing in this region was exponentially reduced to 0.1 nm at the interface. In the lateral direction the mesh lines had a spacing of 250 nm. Close to the source and drain contacts the spacing was exponentially reduced to 1 nm. In the dielectric only a few grid points are necessary, since no charge carriers are present.

To account for interface charge density at the semiconductor-dielectric interface, Q_{if}, which causes a shift of the switch-on voltage, V_{SO}, a thin layer with a fixed space charge density was defined in the dielectric at the interface. The charge density in this layer was calculated by Q_{if}/d_{if}, where d_{if} is the thickness of the charged layer, chosen to be 1 nm. To describe a doped semiconductor, a uniform acceptor doping density was assigned to the semiconductor layer.

Contrary to typical inorganic semiconductors the charge-carrier mobility in organic semiconductors depends on the charge-carrier density. Various temperature, density and field dependent mobility models have been reported [12–18]. Here we assume that the charge transport is described by variable range hopping in an exponential density of localized states (DOS), as described by Vissenberg and Matters [12]. The hole mobility is then given by Eq. 1.2. A similar expression holds for electrons.

The calculated current strongly depends on the boundary conditions at the contacts. Several models for charge injection into organic semiconductors have been reported [19–23]. However, a decisive model is still lacking [24]. In the following description of the contacts we focus on hole injection, but similar processes hold for electrons. In first approximation, we used standard thermionic emission. The energetic barrier for hole injection, φ_B, was taken equal to the energy difference between the workfunction of the metal and the highest occupied molecular orbital (HOMO) energy of the semiconductor, φ_{B0} [25]. Thermionic emission was implemented by defining a fixed hole density at the contact using Boltzmann statistics:

$$p_c = N_V \exp\left(-\frac{\varphi_B}{k_B T}\right) \tag{3.4}$$

where N_V is the effective density of states of the valence band, which was taken equal to the monomer density of about $10^{21}\,\mathrm{cm}^{-3}$. The exact value has negligible influence on the calculated current [4, 7]. For injection barriers smaller than 0.3 eV, the calculated hole current was not injection limited; the contact is then ohmic for holes. Thermal equilibrium is imposed at the contacts, so the electron density at the contact follows from the p–n product as $n_c = N_C \exp[(\varphi_B - E_g)/k_B T]$. The effective density of states of the conduction band, N_C, was taken equal to N_V. The bandgap energy, E_g, is taken as the energy difference between the HOMO and lowest unoccupied molecular orbital (LUMO) of the semiconductor. We note that nc is negligible for a typical bandgap of 2 eV. As a result, the electron injection is strongly suppressed.

For hole-injection barriers larger than 0.3 eV, the current becomes injection limited. Standard thermionic emission is then not sufficient to describe the charge injection, as discussed in Chapter 5. Additional mechanisms such as barrier lowering by the image potential or Fowler-Nordheim tunneling become increasingly important for high barriers and high electric fields [24]. To study charge injection in transistors with a high injection barrier, image potential barrier lowering was included in the calculations. For simplicity further mechanisms are ignored. We implemented a Schottky contact by defining a boundary condition for the hole current, instead of a boundary condition for the hole concentration. The hole current at the contact is then defined as:

$$J_p = \frac{AT^2}{N_V}(p - p_c) \tag{3.5}$$

where A is the effective Richardson constant, p_c is again given by Eq. 3.4. For thermionic emission without barrier lowering, the effective barrier, φ_B, is equal to the initial barrier, φ_{B0}. If image-potential lowering is taken into account, then the effective barrier decreases. The barrier lowering is a function of the electric field at the source contact, E. The resulting effective barrier then reads [26]:

$$\varphi_B = \varphi_{B0} - \Delta\varphi \qquad \text{with:} \qquad \Delta\varphi = e\sqrt{\frac{eE}{4\pi\varepsilon_0\varepsilon_{sc}}} \tag{3.6}$$

To artificially suppress the electron density in the calculations as described in Chapter 6, the quasi-Fermi level for electrons, φ_n, was adjusted. In steady-state calculations, φ_n is solved. To prevent the steady-state we manually fixed φ_n at an arbitrarily high value of 500 V. The electron density is then negligible, as it follows from the Boltzmann relation, given by:

$$n = n_i \exp\left(\frac{e(\psi - \varphi_n)}{k_B T}\right) \qquad \text{with:} \qquad n_i = \sqrt{N_V N_C}\exp\left(\frac{-E_g}{2k_B T}\right) \tag{3.7}$$

where n_i is the intrinsic carrier density, which is about $1.6 \times 10^4\,\mathrm{cm}^{-3}$ at 295 K for a semiconductor with a typical bandgap of 2 eV.

3.2 Analytical transport calculations

An analytical model simplifies the calculations, at the cost of additional approximations. Analytical descriptions for the charge transport in disordered organic field-effect transistors have been reported [27–29]. The derivation typically starts with the gradual channel approximation, similar to the derivation of the standard metal-oxide-semiconductor (MOS) equations, as mentioned in Chapter 1 [30]. The field lateral and the field perpendicular to the channel are then assumed to be independent. Contact resistances are ignored and the acceptor density in the semiconductor is disregarded. In the standard MOS equations the carrier mobility is taken constant, but in organic semiconductors the mobility depends on the local

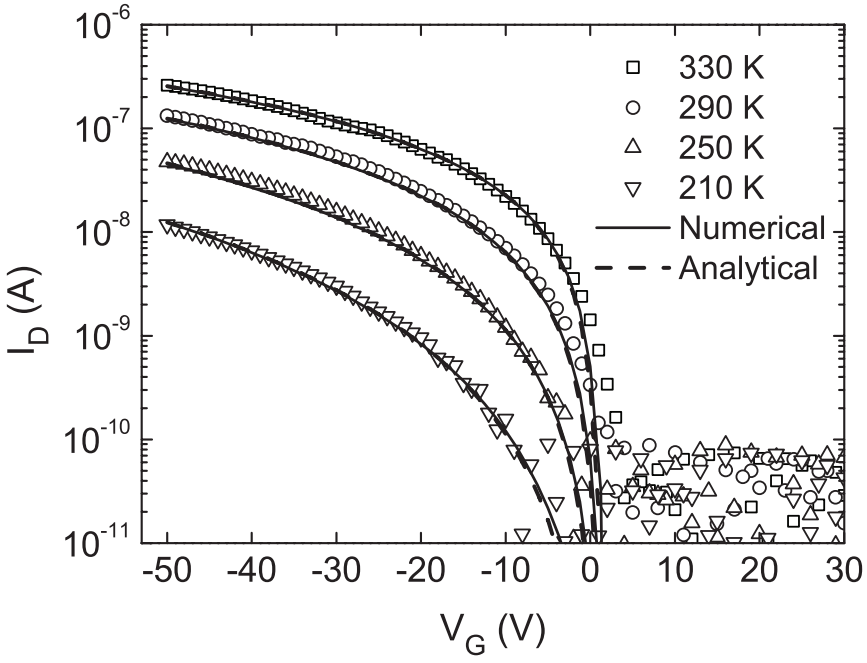

Figure 3.2. Transfer curves of an MDMO-PPV transistor as a function of temperature measured at a drain bias of −2 V. The measurements (symbols) are plotted together with the numerically calculated (solid lines), and analytically calculated currents according to Eq. 3.12 (dashed lines).

carrier density. Therefore, the carrier distribution has to be included explicitly.

In Chapter 8 and 9 of we follow the analytical approach reported by Smits et. al. [29]. Here we present the derivation of their resulting expression for the drain current. The spatial distribution of accumulated charges in the channel was calculated for an exponential DOS, characterized by T_0, using Poisson's equation [31, 32]. An infinite semiconductor thickness, d_{sc}, is assumed. For a p-type transistor, the hole density in the y-direction (perpendicular to the channel), at a point x between the source and drain (along the channel) is then given by:

$$p(V_x, y) = \frac{2\varepsilon_0 \varepsilon_{sc} k_B T_0}{e^2 (y + y_0)^2} \tag{3.8}$$

with

$$y_0(V_x) = -\frac{2\varepsilon_0 \varepsilon_{sc} k_B T_0}{e C_i V_x}$$

where V_x is the difference between the gate bias and the local channel potential at point x in the channel. Calculations of the effective accumulation layer thickness show that it is typically a few nanometers. Equation 3.8 shows that the charge car-

rier density decreases with the distance squared from the semiconductor-dielectric interface. We assume that the charge transport is described by variable range hopping in an exponential DOS, as described by Vissenberg and Matters [12]. The local mobility as a function of V_x and y is then found by inserting Eq. 3.8 into Eq. 1.2. Next, the sheet conductance at position x, $G_{sh}(V_x)$, can be calculated by integrating over the semiconductor layer thickness:

$$G_{sh}(V_x) = \int_0^{d_{sc}} ep\mu(p)\, dy \tag{3.9}$$

The drain current can now be calculated by using the fact that the current is constant through each y, z-plain:

$$I_D = -WG_{sh}(V_x)\frac{\partial V_x}{\partial x} \tag{3.10}$$

and integration over the channel length:

$$\int_0^L I_D dx = I_D L = -W \int_0^L G_{sh}(V_x)\frac{\partial V_x}{\partial x} dx \tag{3.11}$$

The source–drain current eventually follows as [29]:

$$\begin{aligned} I_D &= f\frac{W}{L}\left(\frac{1}{2k_B T_0 \varepsilon_0 \varepsilon_{sc}}\right)^{\frac{T_0}{T}-1} {C_i}^{\frac{2T_0}{T}-1} \frac{T}{2T_0}\frac{T}{2T_0 - T} \\ &\quad \times\left(\|V_{SO} - V_G\|^{\frac{2T_0}{T}} - \|V_{SO} - V_G + V_D\|^{\frac{2T_0}{T}}\right) \end{aligned} \tag{3.12}$$

with the prefactor f as described in Chapter 1. The effective gate bias is given by $V_{SO} - V_G$, where V_G is the gate bias and V_{SO} is the switch-on voltage, defined as the gate bias at the onset of accumulation [28]. The capacitance per unit area is indicated by C_i. The notation $\|u\| \equiv \frac{1}{2}(|u| - u)$ is included in Eq. 3.12 to ensure that the calculated current in depletion is zero. The drain current given by Eq. 3.12 has been used to calculate all regimes in unipolar as well as in ambipolar organic transistors [29]. Excellent agreement is obtained between experimental data and numerically as well as analytically calculated curves, as presented in **Fig. 3.2**.

3.3 Acceptor density determination

For an undoped transistor, the threshold voltage, V_t, coincides with the onset of accumulation current, V_{SO}. The switch-on voltage is determined by dipoles and charged states at the semiconductor-dielectric interface. In organic transistors

based on P3HT, p-type doping can be introduced by exposure to an oxidizing gas, as introduced in Chapter 2. As shown in **Fig. 3.3**, the total shift of the threshold voltage upon exposure consists of two distinct voltage shifts: a shift of the switch-on voltage, ΔV_{SO} and of the pinch-off voltage, V_{pinch}. A clear crossover from field-effect accumulation current to a depletion bulk current can be observed. This 'shoulder' shape is due to the carrier dependent mobility [5].

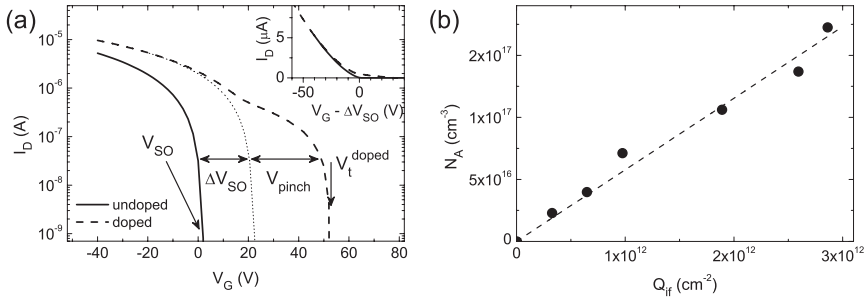

Figure 3.3. (a) Transfer curves of a P3HT field-effect transistor. The P3HT film thickness was 205 nm and the channel width and length were 2500 µm and 10 µm. The transfer curves were measured in the linear regime at a source drain bias of -2 V before and after exposure to an oxidizing gas. The figure shows the definitions of V_t, V_{SO}, ΔV_{SO}, and V_{pinch}. The inset shows the same curves on a linear scale after correction for ΔV_{SO}. (b) The bulk acceptor density N_A versus the calculated surface charge density Q_{if}.

The doping increases the bulk conductivity of the semiconductor. A current will flow in the bulk, additionally to the accumulation channel current. When a positive gate bias is applied, eventually the entire film will be depleted from holes, and no current will flow. The additional gate bias needed to entirely pinch-off the current is referred to as the pinch-off voltage, V_{pinch}. The pinch-off voltage depends mainly on the semiconductor thickness and the doping concentration, N_A. Therefore, the doping concentration can be calculated from V_{pinch}. Assuming a uniform doping profile, N_A follows from [33, 34]:

$$N_A = \frac{V_{pinch}}{e d_{sc}\left(\frac{d_{sc}}{2\varepsilon_0 \varepsilon_{sc}} + \frac{1}{C_i}\right)} \tag{3.13}$$

The switch-on voltage is modeled by introduction of an interface charge density $Q_{if} = -(V_{SO} + \Delta V_{SO})C_{if}/e$. Figure 3.3b shows that Q_{if} scales linearly with N_A. The oxidizing gas oxidizes the semiconductor as well as the dielectric surface, thereby creating interface states. Therefore a linear relation between N_A and Q_{if} can be expected. The ratio depends on the surface coverage of the HMDS, because HMDS passivates the dielectric surface, effectively protecting the surface from the oxidizing gas.

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Carrier-density dependence of the hole mobility in doped and undoped regioregular poly(3-hexylthiophene)

4

Abstract

We investigate the mobility of regioregular poly(3-hexylthiophene) (P3HT) over a carrier-density range from $10^{15}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$. Hole-only diodes were used for densities below $10^{16}\,\mathrm{cm}^{-3}$ and field-effect transistors were used for carrier densities higher than $10^{18}\,\mathrm{cm}^{-3}$. To fill the gap intermediate densities were probed using chemically doped Schottky diodes and transistors. Combination of the mobilities in doped and undoped devices experimentally establishes the full relation of the mobility over the whole carrier-density range.

4.1 Introduction

Solution-processable conjugated polymers such as polythiophene derivatives are attractive candidates for application in low-cost and flexible microelectronic devices. The electrical transport is dominated by thermally assisted intermolecular hopping of the charge carriers. The transport depends on carrier density, temperature and electric field [1–6]. At room temperature and at relatively small electric field the transport is dominated by the carrier-density and the field dependence plays a negligible role [6, 7]. Experimentally capturing the full extent of the relation between mobility and carrier density is necessary for understanding and improving the device performance. For poly(p-phenylene vinylene) derivatives the mobility extracted from diodes is low, around $10^{-7}\,\mathrm{cm}^2/\mathrm{Vs}$, and independent of carrier density. The mobility extracted from field-effect transistors however increases with charge-carrier density up to typically $0.001\,\mathrm{cm}^2/\mathrm{Vs}$. The difference originates from the charge-carrier density, which in diodes is typically $10^{15}\,\mathrm{cm}^{-3}$ to $10^{16}\,\mathrm{cm}^{-3}$ and in transistors from $10^{18}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$ [8]. However, a full mobility carrier-density relation is hindered by a gap in the carrier density between $10^{16}\,\mathrm{cm}^{-3}$ to $10^{18}\,\mathrm{cm}^{-3}$ [8, 9].

Polythiophenes have been extensively applied in field-effect transistors (FET) [10, 11] and solar cells [12]. The benchmark is regioregular poly(3-hexylthiophene) (P3HT). To probe the mobility in the gap of $10^{16}\,\mathrm{cm}^{-3}$ to $10^{18}\,\mathrm{cm}^{-3}$, we deliberately doped P3HT [13]. Doping in organic semiconductors has been an important topic since the introduction of these semiconductors [14, 15]. More recently achievements have been made in the field of stable n-type doping and solution-processed doping [16–18]. In this Chapter, we investigated hole-only diodes, (doped) Schottky diodes and (doped) transistors. In this way over the whole range of charge-carrier densities, the mobility can be unified by a zero-field mobility with a density dependent term based on hopping in an exponential density of states (DOS) [8, 19].

4.2 Results and discussion

Hole-only diodes, Schottky diodes and field-effect transistors were fabricated as described in Chapter 2. Regioregular P3HT, obtained from Imperial College London, was spin-coated from chloroform. After spin-coating P3HT, all devices were annealed at 150 °C for 2 hours in vacuum. To chemically dope P3HT, we exposed the devices to a vapor of trichloro-(1H, 1H, 2H, 2H)-perfluorooctylsilane (TCFOS), as described in Chapter 2 [20].

The current density of a P3HT hole-only diode was measured as a function of applied voltage and is presented in **Fig. 4.1**. The transport was measured as a function of temperature. At low bias the current density scales with the voltage squared, indicating space-charge-limited current (SCLC) with a constant mobility. PEDOT:PSS is an ohmic contact to P3HT, because the work function matches the energy of the highest occupied molecular orbital (HOMO) of P3HT [21]. The transport in the diode is then bulk limited. At high bias the current density is enhanced. Charge transport is due to thermally activated hopping between localized states at the Fermi level. Device simulations were performed by using a numerical

drift-diffusion model [22]. A hopping mobility that depends on both charge-carrier density and electric field was used, as introduced in Chapter 1 as Eq. 1.3 [12, 23]. Figure 4.1 shows that for all temperatures a perfect agreement between measured and calculated current densities is obtained. As fit parameters we used a room temperature zero-field mobility of $1.5 \times 10^{-4}\,\mathrm{cm^2/Vs}$ with an activation energy of about 0.2 eV, a zero-field conductivity of $5 \times 10^{6}\,\mathrm{S/m}$, a characteristic temperature for the exponential DOS, T_0, of 475 K and an overlap parameter α^{-1} of 3 Å. The numbers agree well with reported values for P3HT [8]. We note that at room temperature and for the low applied bias the density dependence dominates and the electric field dependence is negligible. To extract from the fit the charge-carrier density versus mobility relation we used the procedure reported by Tanase et.al. [9, 24]: The average mobility can be estimated as $\mu_{undoped} = JL^3/(1.2\varepsilon_0\varepsilon_{sc}V^2)$ and the average density as $p_{undoped} = 1.5\varepsilon_0\varepsilon_{sc}V/(eL^2)$. Both are a function of the applied bias, and therefore an average density and mobility can be calculated for each current-voltage data point. The mobility is presented later as a function of average charge density in **Fig. 4.4**.

In order to increase the charge-carrier density we fabricated doped Schottky diodes. As a reference however, first undoped diodes were investigated. The Schottky diodes exhibit a rectification of more than 6 orders of magnitude. The current in forward bias is presented in **Fig. 4.2a**. The current density is calculated with the same numerical model as for the hole-only diodes, using identical fit parameters. The solid line in Fig. 4.2a shows that a good agreement between calculated and measured current densities is obtained. After the undoped Schottky diodes were characterized, the diodes were doped. Exposing P3HT to vaporized TCFOS

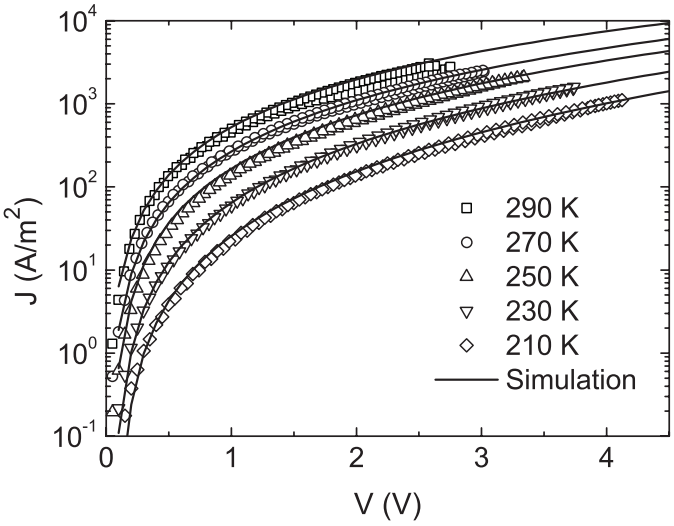

Figure 4.1. Current density versus applied bias for a P3HT hole-only diode with a thickness of 135 nm, measured as a function of temperature. The solid lines represent the fit according to the carrier-density-dependent and field-dependent mobility model.

yields p-type doping [13, 20]. Figure 4.2a shows that the current density in forward bias increases. The origin is a combination of the increased carrier density, plus an increase in mobility due to the higher density. To quantify the relation we determined the charge-carrier density independently from capacitance-voltage (C–V) measurements in reverse bias. We followed a literature procedure as presented previously in [18]. An AC voltage of 100 mV was superimposed to the applied reverse DC bias and a frequency scan was made from 10 Hz to 20 MHz at each bias. By modeling the diode as a parallel RC circuit for the depletion region in series with another RC circuit for the semiconductor bulk, the capacitance of the depletion region, C_P, was extracted. In Fig. 4.2b, C_P^{-2} is plotted versus reverse bias for a diode exposed 20 minutes to TCFOS vapor. A straight line was obtained and the acceptor density N_A was calculated from the slope as [18]:

$$N_A = \frac{-2}{e\varepsilon_0\varepsilon_{sc}} \left(\frac{d\left(C_P{}^{-2}\right)}{dV_{DC}} \right)^{-1} \tag{4.1}$$

The extracted value was then used as input to calculate the forward current density. The solid line in Fig. 4.2b shows that a good agreement is obtained. From the calculation the corresponding average mobility is extracted. For three doped Schottky diodes the mobility is presented as a function of charge-carrier density in Fig. 4.4.

To probe the mobility at high carrier density, field-effect transistors were investigated. The carrier density decreases with the distance squared from the semiconductor-dielectric interface. The density at the interface dominates the transport and was calculated as a function of gate bias as described in Chapter 3, Eq. 3.8 [25]. The linear mobility was approximated at each gate bias from Eq. 1.6. Contact resistance was neglected, since the Au contacts make an ohmic contact for holes with the semiconductor, as discussed in the next Chapter. The extracted mobility versus density for an undoped P3HT transistor is shown in Fig. 4.4.

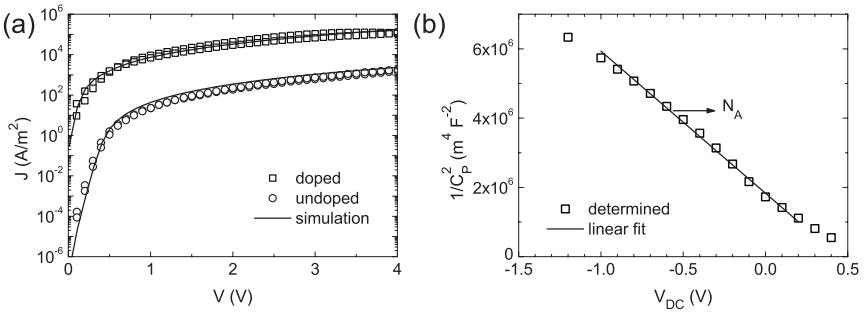

Figure 4.2. (a) Current density versus voltage of an undoped and a doped Schottky diode with a thickness of 195 nm. The solid lines represent the fit according to the model. (b) The inverse of the capacitance squared versus DC bias of the doped Schottky diode. The solid line represents a linear fit.

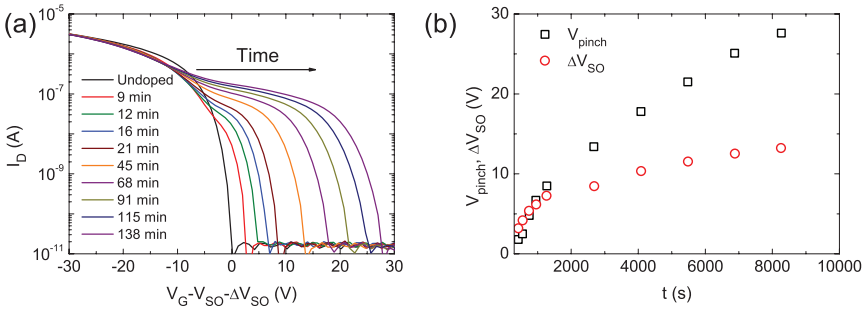

Figure 4.3. Transfer curves in the linear regime of a P3HT field-effect transistor in vacuum before and after exposure to TCFOS vapor at room temperature, for different exposure times. The channel length and width were 10 µm and 2500 µm, and the semiconductor thickness was 100 nm. The drain bias was −2 V and the transfer curves are corrected for the shift in switch-on voltage with respect to the pristine undoped transistor at $t = 0$ [20]. The switch-on voltages range from 5.8 V for the undoped transistor to 19 V after 138 min.

Exposing the transistors to TCFOS vapor leads to doping of P3HT. The doping density can be varied by changing the exposure time. Transfer curves recorded in-situ at different exposure times are presented in **Fig. 4.3a**. A shoulder appears in the transfer curve; a higher positive bias is needed to deplete the doped bulk semiconductor and pinch-off the channel. Also the on-current at negative gate bias, in accumulation, slightly increases due to a shift in switch-on voltage. The switch-on voltage, defined as the on-set of the channel current at flatband [26], shifts to positive values upon doping. The shift in switch-on voltage is presented as a function of exposure time in Fig. 4.3b. Each transfer curve in Fig. 4.3a is corrected for its switch-on voltage, indicating that the accumulation currents are identical within experimental error. The corrected transfer curves show a cross-over from an accumulation mode into a bulk depletion mode transistor [20, 27]. The current in accumulation is dominated by the channel current, while in depletion, at positive gate bias, the current is mainly flowing through the bulk semiconductor. The doping density can be calculated from the pinch-off voltage, plotted in Fig. 4.3b as a function of exposure time. The mobility can be calculated from the current at the switch-on voltage, as described in Chapter 3 [20, 27]. The extracted mobilities and carrier densities are presented in Fig. 4.4 as well.

The extracted mobility versus extracted charge-carrier density from all the investigated devices are presented in Fig. 4.4. The gap between the undoped diodes and undoped transistors is probed with the doped diodes and the doped transistors. Moreover, Fig. 4.4 shows that the hole mobility flattens for charge-carrier densities below $10^{16}\,\mathrm{cm}^{-3}$ and increases as a power law for higher charge densities. The power-law dependence is due to hopping transport in disordered semiconductors [12, 19]. Slight deviations from the power law at intermediate density might be due to anisotropy in the charge transport caused by the nano-crystalline nature of P3HT.

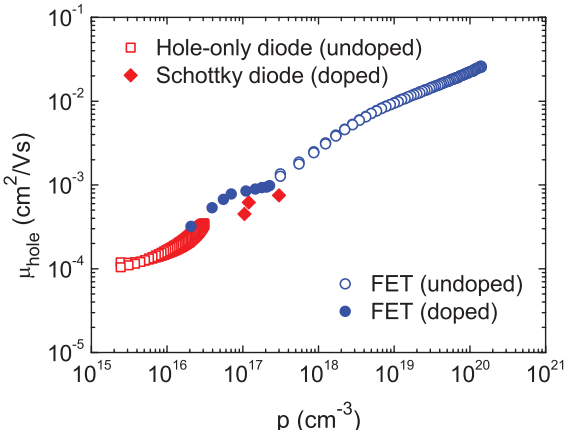

Figure 4.4. Charge-carrier mobility versus carrier density of P3HT, as extracted from undoped hole-only diodes, doped Schottky diodes, and undoped and doped field-effect transistors.

4.3 Summary

We have experimentally probed the charge-carrier mobility as a function of carrier density for P3HT over a wide density range. The mobility at low, $10^{15}\,\mathrm{cm}^{-3}$ to $10^{16}\,\mathrm{cm}^{-3}$, and high, $10^{18}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$, carrier density was extracted from undoped hole-only diodes and field-effect transistors, respectively. The room temperature mobility is nearly constant at densities below $10^{16}\,\mathrm{cm}^{-3}$, whereas the mobility increases with a power law for densities higher than $10^{18}\,\mathrm{cm}^{-3}$. The mobility at intermediate density has been probed by chemically doped Schottky diodes and transistors and unites the low- and high density regimes.

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Gate-bias assisted charge injection in organic field-effect transistors

5

Abstract

In the previous Chapter, ohmic contacts were used. Contact resistance or charge injection barriers have been neglected, which might lead to a severe underestimation of the extracted mobility, in certain cases. Therefore, it is necessary to quantify under which circumstances the injection barrier does play a role. This question will be addressed in the following Chapter. The charge injection barriers in organic field-effect transistors (OFETs) seem to be far less critical as compared to organic light-emitting diodes (OLEDs). Counter intuitively, we show that the origin is image-force lowering of the barrier due to the gate bias at the source contact, although the corresponding gate field is perpendicular to the channel current. In coplanar OFETs, injection barriers up to 1 eV can be surmounted by increasing the gate bias, enabling extraction of bulk transport parameters in this regime. For staggered transistors, however, the injection is gate-assisted only until the gate bias is screened by the accumulation channel opposite to the source contact. The gate-assisted injection is supported by two-dimensional numerical charge transport simulations that reproduce the gate-bias dependence of the contact resistance and the typical S-shaped output curves as observed for OFETs with high injection barriers.

5.1 Introduction

The current in an organic light-emitting diode (OLED) strongly depends on the charge injection barrier [1–5]. The injection barrier is taken as the energy difference between the work function of the electrode and the highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO) energy of the organic semiconductor. When the barrier is less than about 0.25 eV, the current is bulk limited [5]. In that case, the maximum current that is electrostatically allowed is the space-charge limited current. When the injection barrier is larger than 0.25 eV the current is injection limited, the bulk current cannot be supplied by the contact. The diode current typically decreases by an order of magnitude for each 0.25 eV increase in barrier height [6]. Hence to maximize the current and efficiency in OLEDs matching between the work function of the electrode and the HOMO or LUMO energy of the semiconductor is crucial.

In organic field-effect transistors (OFETs) the nature of the contact seems less important. There are numerous examples showing that the charge transport in transistors is rather tolerant for injection barriers. Pentacene has been investigated using transistors with source and drain electrodes with widely different work functions: Au, Cu, Ni. Surprisingly, the saturated output currents differed by less than an order of magnitude [7]. Extreme examples are ambipolar transistors, using a single electrode material to inject both electrons and holes, where considerable current is measured even with injection barriers larger than 0.5 eV [8–10].

In OFETs the contact resistance depends on the barrier height at the metal-semiconductor interface, but it also strongly dependents on the biases, the transistor architecture and geometry. In particular, the contact resistance reduces with increasing gate bias [7, 11–13] and with increasing temperature [14, 15]. Severely contact limited transistors show an S-shaped output curve (current vs. drain bias, I_D versus V_D), with a nonlinear diode-like behavior at low drain bias [12, 14, 16, 17]. Coplanar transistors usually have a higher contact resistance with respect to their staggered counterpart [16]. In staggered transistors the contact resistance was attributed to the current-crowding effect and to a gate-dependent bulk resistance [18–20]. In a coplanar structure the contact resistance has been explained as the combined effect of a Schottky contact and a field-dependent mobility [21, 22]. Although these physical effects enable a good modeling of the transistor characteristics, they are not able to explain why an OFET is more insensitive to the barrier height than an OLED [11–13].

In this Chapter, we show that the observed difference between charge injection in an OLED and in an OFET is implicitly due to the gate bias. A quantitative analysis of the charge transport requires a model to describe the charge injection into a disordered organic semiconductor. Various models have been reported [21, 23–26], but a final consensus has not yet been reached. As a first order approximation we use thermionic emission [27]. We show that by including image-force lowering the tolerance of charge transport in an OFET to the injection barrier can be quantitatively explained. Transfer and output curves are reproduced and the consequences for parameter extraction are discussed. Coplanar and staggered OFETs with the same geometrical and physical parameters are analyzed and compared.

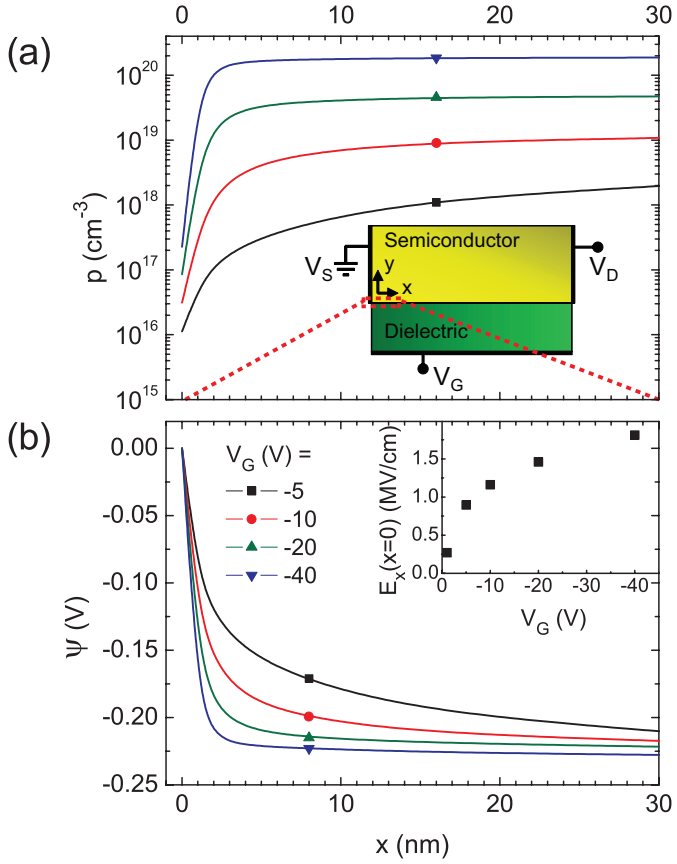

Figure 5.1. (a) hole density and (b) local electrostatic potential, ψ, in the channel of an injection limited p-type bottom-contact bottom-gate (coplanar) transistor with an initial injection barrier $\varphi_{B0} = 0.5$ eV. Density and potential are plotted versus distance from the source contact, x, at the semiconductor-dielectric interface, as a function of gate bias. Inset in (a): schematic representation of a bottom-contact bottom-gate field-effect transistor. Inset in (b): the electric field in the x-direction at the source contact, at the dielectric interface, versus gate bias. The drain bias was -2 V, the channel length and width were 20 µm and 1000 µm, the hole mobility was 0.01 cm^2/Vs, the effective Richardson constant was 100 AK^{-2}cm^{-2}, and the gate capacitance was 17 nFcm^{-2}.

5.2 Results and discussion

We take a unipolar p-type field-effect transistor with an undoped semiconductor, i.e. we assume a background doping density not higher than $10^{16}\,\mathrm{cm}^{-3}$ [28], as shown in the inset of **Fig. 5.1a**. At zero gate bias the OFET can basically be considered as a lateral OLED. The source-drain bias of typically a few volts is distributed over the channel with a typical length of a few micrometer. As a result the source-drain field in an OFET is typically 2–3 orders of magnitude lower than the electric field in an OLED. Due to the much lower electric field, the associated image-force lowering can be neglected, the injection barrier is then equal to the difference between the electrode work function and the HOMO energy of the semiconductor. In p-type OFETs the source is grounded, whereas the drain is operated at a small negative bias. Consequently, holes are injected from the source contact. The energy barrier at the drain contact can be disregarded since for hole extraction this barrier does not play a role, as also demonstrated by scanning Kelvin probe potentiometry measurements [29].

To investigate the role of the gate bias on the charge injection, we calculated the carrier density, electric potential, and the resulting current in a p-type transistor. To quantify the injection by the source contact, we implemented classical thermionic emission by defining the boundary condition for the hole current as described in Chapter 3. The current is then defined as: $J_p = \frac{AT^2}{N_V}(p - p_c)$, where A is the effective Richardson constant, T the absolute temperature, N_V the effective density of states in the semiconductor and p the hole density. The equilibrium hole density depends on the effective barrier for holes, φ_B, and it is given by: $p_c = N_V \exp(-\varphi_B/k_BT)$ where k_B is the Boltzmann constant. For thermionic emission without barrier lowering, the effective barrier, φ_B, is equal to the initial barrier, φ_{B0}: the energy difference between the electrode work function and the HOMO energy. If image-force lowering is taken into account, then the effective barrier decreases. The barrier lowering is a function of the electric field at the source contact, E, and reads [27]: $\Delta\varphi = e\sqrt{\frac{eE}{4\pi\varepsilon_0\varepsilon_{sc}}}$, where $\varepsilon_0\varepsilon_{sc}$ is the semiconductor permittivity and e is the elementary charge.

In order to model the hole injection we used the 2D device simulator CURRY [30–32], as introduced in Chapter 3. Thermionic emission in combination with image-force lowering was implemented. We note that at low temperatures or at very high electric fields additional injection mechanisms such as thermally-assisted tunneling or Fowler-Nordheim tunneling might be operative [29]. For simplicity these mechanisms are disregarded. Furthermore, in order to disentangle gate-bias assisted injection from effects due to a field- and density dependent mobility we use a constant mobility in this Chapter. In this sense our approach differs from [21], where the interdependence of contact properties and field- and density-dependent mobility in OFETs has been studied but unfortunately barrier lowering was neglected. It is worth noting that, in general, both Schottky barrier lowering and the field- and density-dependent mobility can contribute to contact effects.

In order to elucidate the role of V_G on the charge injection, we start our analysis considering a bottom-contact bottom-gate OFET, as schematically depicted in the inset of Fig. 5.1a. The local hole density and potential as a function of the distance

from the source contact are plotted for different V_G, in Fig. 5.1, in equilibrium. When a gate bias is applied, holes with a concentration of $C_i V_G$, with C_i the gate capacitance per unit area, are accumulated in the channel, which becomes conductive. However, due to the injection barrier the hole concentration strongly drops close to the source contact and a depletion region is formed, as shown in Fig. 5.1a. As a result the source-drain bias mainly drops over this depletion region at the source contact. For increasing gate bias, the depletion region narrows, as shown in Fig. 5.1b. This can be explained as follows: The depletion width depends on the charge carrier concentration in the semiconductor, that is modulated by the gate bias according to $C_i V_G$. A higher V_G thus gives a larger concentration, thereby reducing the depletion width of the reverse-biased Schottky diode. As shown in the inset of Fig. 5.1b the reduction of the width of the space-charge region is accompanied by an increase of the lateral electric field at the contact, E_x. Hence, the effective barrier lowers by the image force effect and the injected current is higher. A smaller part of the drain-source bias, V_D, drops over the contact. In principle, by applying a large enough gate bias, the field will be eventually high enough to supply the current demanded by the bulk. We note that the injection limited curves will never completely reach the bulk limited curve, because a small part of V_D will always drop over the contact. In summary, the electric field at the source contact is responsible for the barrier lowering and the field is implicitly modulated by the gate bias.

Transfer curves calculated without image-force lowering as a function of initial barrier height are presented in **Fig. 5.2a**. For the calculations we took a typical value for the channel length of 20 µm. For much larger channels the bulk channel resistance is dominant and at much smaller lengths short-channel effects might dominate [33–36]. The analysis of short channel effects is beyond the scope of this work. As expected, for barriers up to 0.3 eV the calculated transfer curves are identical, the current is bulk limited. At higher barriers the current becomes injection limited. The current decreases exponentially with increasing barrier height, about 60 mV/decade. This value differs from the experimental value derived from OLEDs, 250 mV/decade, presumably due to the incorrect assumption of thermionic emission as the dominating injection mechanism. A model based on thermally assisted hopping from the electrode into the localized states of the organic semiconductor, which are broadened due to disorder, is probably more realistic [26], but mathematically hard to implement in the 2D device solver. The thermionic emission implemented here leads to a similar basic understanding of the gate-bias assisted injection process in OFETs.

Without image force lowering the transfer curves saturate with increasing gate bias, as shown in Fig. 5.2a. As a comparison, transfer curves calculated including image-force lowering are presented in Fig. 5.2b. At low gate bias, the calculated current strongly depends on the initial barrier height, similar to the OLED case. However, as the gate bias increases, the calculated currents almost converge due to the gate-bias assisted image-force lowering. Hence at low gate bias the current is injection limited, while at high bias the current becomes bulk limited. This indicates that in the case of bottom-contact bottom-gate transistors the mobility values extracted in the linear regime at high gate bias approach the bulk value.

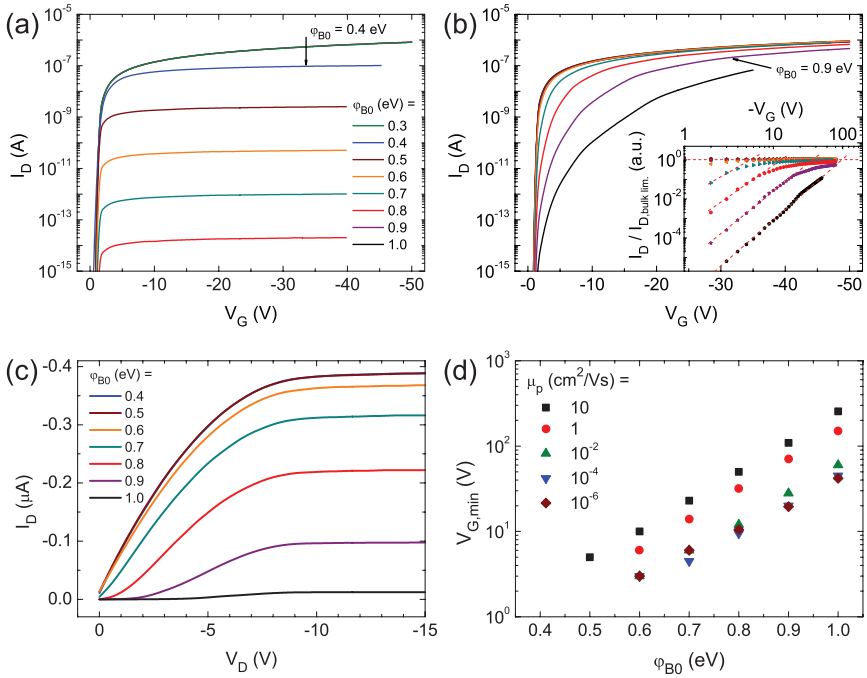

Figure 5.2. Simulated transfer curves of a *p*-type bottom-contact bottom-gate (coplanar) transistor as a function of initial injection barrier, at a drain bias of −2 V. The calculations were performed (a) without and (b) with image-force barrier lowering at the source contact. Inset in (b): The current at each gate bias normalized to the bulk-limited current, obtained for zero barrier, at the corresponding bias. The dotted lines are a guide to the eye. (c) Calculated output curves, including image-force lowering, as a function of the initial injection barrier at the source, φ_{B0}, at $V_G = -10$ V. (d) The calculated gate bias required to overcome the injection barrier, $V_{G,min}$, versus the initial injection barrier, φ_{B0}, as a function of the hole mobility, μ_p. The drain bias was −2 V. The parameters such as bulk mobility, capacitance, channel length and width are identical to those of Fig. 5.1.

Furthermore, the contact resistance for a given barrier height can be calculated from Fig. 5.2b. For instance at large barriers we can ignore the bulk channel resistance. The contact resistance is then approximately equal to the drain bias divided by the drain current. Figure 5.2b therefore indicates that the contact resistance drops with gate bias, in good agreement with literature data [7, 11–13]. Thus, without barrier lowering the effective barrier is equal to the initial barrier independent of the gate bias. Hence, the transfer curves saturate and do not converge. When barrier lowering is taken into account the effective barrier decreases with increasing gate bias. Hence the difference in calculated currents gets smaller, and at very high gate bias the calculated currents converge.

The role of the drain-source bias is elucidated in Fig. 5.2c, where the output curves are presented as a function of initial barrier height. The output currents are

calculated including image-force lowering. It appears that for barriers up to 0.5 eV the calculated curves are identical. At low drain bias the current increases linearly with drain bias, the extracted mobility is constant and equal to the nominal bulk mobility. With increasing barrier height, the current has a superlinear, diode-like dependence on V_D at low drain bias and the current is almost perfectly flat at large drain bias. Consequently, the output curves at high barrier height show an S-shape, as experimentally observed in severely contact-limited transistors [12, 14, 16, 17]. The origin is that for a given gate bias the barrier lowering increases with source-drain bias, since the total field at the source contact is enhanced. The S-shape has previously been attributed to an electric field dependent mobility [21, 22]. Here we show that a large injection barrier described by thermionic emission and image-force lowering alone is sufficient. We note that calculations without barrier lowering only result in a reduced current, but not in a different shape.

In the limit of infinite gate bias, all injection barriers in a coplanar transistor can be surmounted, as shown in Fig. 5.2b. Practical questions are: What is the minimum gate bias needed to overcome the barrier, $V_{G,min}$? And how does this bias depend on the bulk mobility? To estimate the minimum gate bias we replot the transfer curves on a double logarithmic scale as shown in the inset of Fig. 5.2b. The current is normalized to the bulk current as calculated without injection barrier. Hence for barriers below about 0.3 eV a straight line at unity is obtained. For higher barriers the current at low bias is injection limited, and an apparent power law dependence is obtained. The intersection of the extrapolated power law with the bulk normalized current is taken as $V_{G,min}$. The values derived are presented in Fig. 5.2d as a function of initial barrier height. At low barrier height the minimum gate bias is negligible. The minimum gate bias is calculated to increase almost exponentially with barrier height, which is expected from the exponential dependence of the thermionic emission on injection barrier height.

As an example, Fig. 5.2d shows that for low-mobility semiconductors, μ_p lower than about $10^{-2}\,\mathrm{cm}^2/\mathrm{Vs}$, barriers of for instance 0.8 eV can be overcome at a gate bias of about 10 V. This indicates that the mobility values extracted at higher gate biases approach the bulk value. Mobility values extracted at low bias can be orders of magnitude lower. We note that in an OLED the mobility cannot reliably be extracted for high injection barriers without having a detailed knowledge on the injection mechanism. Figure 5.2d shows that for high-mobility semiconductors a higher minimum gate bias is needed to overcome a similar barrier. In fact, an increased mobility results in a higher channel current, which has to be supplied by the contact. The analysis suggests that although much research effort is directed towards high-mobility materials, the best performance can only be achieved with a good balance between charge injection and current transport.

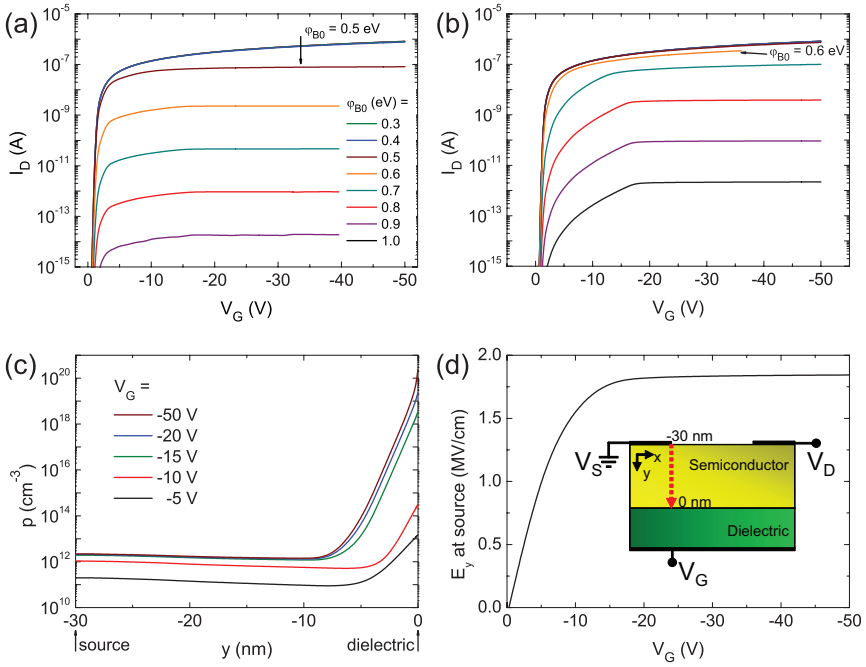

Figure 5.3. Simulated transfer curves of a p-type top-contact bottom-gate (staggered) transistor as a function of initial injection barrier, at a drain bias of -2 V. The calculations were performed (a) without and (b) with image-force barrier lowering at the source contact. (c) Hole density along the vertical y-direction at the source contact, along the red dashed line in the inset in (d), with an initial barrier $\varphi_{B0} = 0.8$ eV. (d) The electric field in the y-direction at the source contact, versus the gate bias. Inset: Schematical representation of a top-contact bottom-gate field-effect transistor. The width of the source and drain electrodes is 2 µm and all the other parameters not specified, such as the bulk mobility, gate capacitance, channel length and width, are identical to those of Fig. 5.1.

In order to investigate the role of the transistor geometry in gate-bias assisted injection we extend the analysis to the case of staggered top-contact bottom-gate OFETs. The transistor structure is shown in the inset of **Fig. 5.3d**. The channel width and length and the physical parameters of the semiconductor are identical to those used for the coplanar OFET discussed above. The width of the source and drain electrodes is 2 µm. Transfer curves calculated without image-force lowering as a function of the initial barrier height are presented in Fig. 5.3a. For barriers up to 0.4 eV the calculated transfer curves are identical and the current is bulk limited. At higher barriers the current becomes injection limited. It is worth noting that the bulk-limited transfer curves obtained for the staggered OFET (Fig. 5.3a) are identical to those calculated for the coplanar OFET in Fig. 5.2a; the curves have the same magnitude and shape. In the case of the staggered structure, the barrier height after which the current becomes injection limited is slightly higher than the one obtained for the coplanar transistor. This is because in staggered OFETs, with the gate and electrodes on opposite sides of the semiconductor, the effective injection region is a few orders of magnitude larger than for coplanar OFETs, where the injection region is only the side of the contact next to the nanometer-scale transport channel.

Calculated transfer curves including image-force lowering are presented in Fig. 5.3b. For the staggered geometry the current is injection limited for barriers higher than 0.6 eV. Comparing the results plotted in Fig. 5.3a and Fig. 5.3b, the calculated current including barrier lowering becomes injection limited at higher barriers. This confirms that the gate bias also has a beneficial effect on the charge injection in staggered transistors. At small gate bias the current strongly increases with V_G, whereas after a certain value of the gate bias ($|V_G| > 15$ V in Fig. 5.3b) it becomes independent of V_G. This agrees with the results reported in [20]. However, the gate-assisted injection is much weaker than in the coplanar transistor and a nearly ohmic injection cannot be achieved at very high values of V_G. In order to investigate this point, we plot in Fig. 5.3c the hole concentration along the vertical direction at the source as a function of gate bias. For small values of V_G ($|V_G| < 15$ V) the hole concentration at the metal-semiconductor interface is modulated by the gate bias, which explains the strong current increase with V_G in Fig. 5.3b. However, for high gate bias, the accumulated charge at the semiconductor-dielectric interface screens the gate bias. This screening results in a constant hole concentration at the source contact, at the opposite side of the semiconductor, in agreement with previously reported electrostatic simulations [37].

The electric field at the injecting source contact as a function of the gate bias is presented in Fig. 5.3d. When $|V_G|$ is larger than about 20 V, the gate bias is screened by the accumulated channel and the field at the contact remains constant. Therefore, we can conclude that in staggered OFETs the injection is gate-bias assisted until the channel opposite to the source contact is fully accumulated. How effective the screening is depends on the semiconductor thickness. By varying the semiconductor thickness, we verified that the gate-assistance is less pronounced for thicker layers. The analysis physically explains why the contact effects are different in coplanar and staggered transistors. The underlying physics is basically the same, but the role of the injecting contact depends strongly on the transistor geometry.

5.3 Summary

In an OLED the injection barrier should be below 0.3 eV to achieve bulk limited transport. In contrast, an OFET is much more tolerant for injection barriers. The origin is image-force lowering of the barrier due to the high electric field at the source contact. In a coplanar OFET under accumulation the electric field at the source contact progressively increases with increasing gate bias. At low gate bias the source contact limits the injection. However, by increasing the gate bias injection barriers up to 1 eV can be surmounted and extracted parameter values resemble those of the bulk semiconductor. 2D numerical simulations reproduce the typical S-shaped output curves of OFETs with high injection barriers without any further assumptions. In a staggered OFET the injection is gate-bias enhanced until the accumulated channel, opposite to the source contact, screens the gate bias.

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Formation of inversion layers in organic field-effect transistors

6

Abstract

The injection barrier for electrons in *p*-type OFETs is larger than 1 eV, for which the results of Chapter 5 predict severe limiting of the carrier injection. An inversion current in unipolar organic field-effect transistors is not observed, which can be due to trapping of electrons or to negligible electron injection. In this Chapter, we distinguish between both cases by studying the depletion current of unipolar *p*-type transistors based on a deliberately doped organic semiconductor. For each doping level, the current can be completely pinched off, which unambiguously shows that no inversion layer is formed. Numerical calculations show that for electron injection barriers > 1 eV the transistor is thermodynamically not in equilibrium, such that a steady-state is not reached in the time frame of the experiment.

6.1 Introduction

Organic field-effect transistors (OFETs) are being investigated for their use in high-volume applications such as radio frequency identification tags, pixel engines in active matrix displays and sensors [1–4]. In silicon based electronic circuits complementary metal-oxide-semiconductor (CMOS) logic is applied, for which both p-type and n-type transistors are required. The advantages over unipolar logic are low power dissipation and robust operation [5]. In contrast to silicon many organic semiconductors are unipolar, in the sense that the hole conduction is significantly larger than the electron conduction. The electron current is reduced by traps, with typically densities of about $10^{17}\,\mathrm{cm}^{-3}$ [6]. As a result most organic transistors are normally-ON unipolar p-type transistors. Holes are accumulated at negative gate bias resulting in an accumulation current between the source and drain electrode. At positive gate bias, however, the measured current is negligible. Holes in the semiconductor are depleted, eliminating the hole current. Since the total current is the sum of the electron and hole current, the electron current is also negligible.

The absence of an electron current is remarkable: Theoretically, semiconductor physics predicts in steady-state both depletion of holes and inversion, i.e. accumulation of electrons at the semiconductor-dielectric interface. Inversion should always occur since the formation of a negatively charged layer at the semiconductor-dielectric interface, that screens the electric field of the positively biased gate electrode, is energetically the most favorable situation. The fundamental question arises whether the absence of electron current in OFETs is due to trapping of electrons or to the fact that the steady-state is not reached. In the first scenario electrons are injected from the contacts, but are immobilized either in the bulk of the semiconductor or at the semiconductor-dielectric interface. Trapping in the bulk of the semiconductor is unlikely, since the charge carrier densities in OFETs are in the range of $10^{19}\,\mathrm{cm}^{-3}$, two orders of magnitude higher than the bulk electron trap density. Therefore, at these densities all the bulk electron traps are filled and do not play a role in the transport. However, it has been demonstrated by Chua et al. that also severe trapping of electrons at the semiconductor occurs, due to the presence of hydroxyl groups [7]. As a result, the electron current is negligible, regardless of the electron mobility in the bulk. In the second case the rate of electron injection and generation is too low. Many OFETs make use of Au source and drain contacts, that due to their high work function are good hole injectors, but poor electron injectors. The very large injection barriers do not supply the amount of electrons required to form an inversion layer. The steady-state is not reached within the time scale of the DC measurements. The electron current then is negligible because the inversion channel has not been formed yet.

In this Chapter, we distinguish between both cases using unipolar p-type transistors based on a deliberately doped organic semiconductor. By doping the semiconductor, mobile holes are induced, resulting in a measurable bulk current. A positive applied gate bias depletes the holes from the semiconductor. However, if inversion sets in, the gate bias is screened by the (trapped) electrons at the interface. Further increase of the gate bias results in stronger inversion, but not in further depletion of the bulk of the semiconductor. Full depletion of the bulk

is only possible if the gate bias is not screened by an inversion layer. Hence the occurrence of an inversion layer, formed by either mobile or trapped electrons at the semiconductor-dielectric interface, can be inferred from the observation of the depletion current at positive gate bias. Numerical two-dimensional (2D) charge transport simulations were used to calculate the electron and hole distributions without making a priori assumptions on the profiles. The screening dynamics can artificially be introduced by either including or suppressing electrons in the software.

6.2 Results and discussion

Transistors with a bottom-gate bottom-contact configuration were fabricated as described in Chapter 2 [8]. As a semiconductor, regio-regular poly(3-hexylthiophene) (P3HT) was selected to allow comparison of electrical transport with literature reports [8, 9]. To minimize the influence of short-channel effects and contact resistances, channel lengths larger than 10 µm were used. At negative gate bias, holes are accumulated and form a *p*-type conducting channel. Linear transfer curves measured as a function of temperature are presented in **Fig. 6.1**. The current increases both with increasing temperature and gate bias. The hysteresis is negligible and no current is measured for positive gate bias.

The transfer curves were modeled numerically, using the 2D device simulator CURRY [10–12]. Electrical conduction in organic semiconductors occurs by thermally activated hopping of charge carriers between localized states. We approxi-

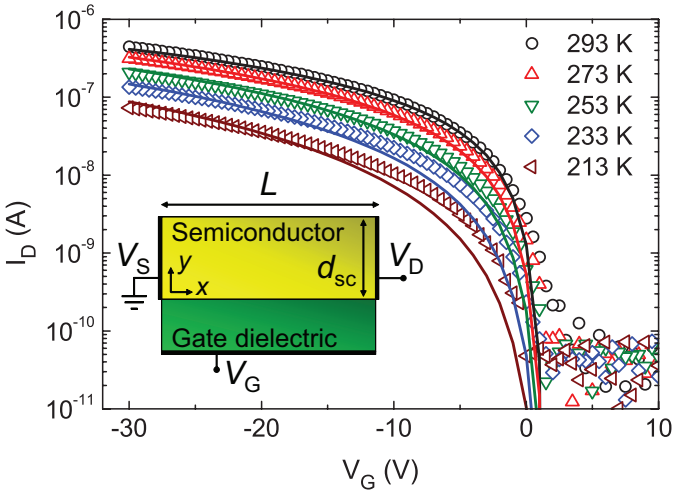

Figure 6.1. Linear transfer curves of a P3HT transistor as a function of temperature, measured at a drain bias of −2 V. Experimental data are represented by symbols and the numerical simulations by solid lines. The channel width and length are 1000 µm and 40 µm. The inset shows a schematic representation of a bottom-gate bottom-contact transistor.

mated the density of localized states (DOS) by an exponential DOS [13]. The local mobility then increases as a power law with charge-carrier density as described in Chapter 1, according to Eq. 1.2. The boundary conditions strongly influence the calculated current. A detailed description of the charge injection is beyond the scope of this Chapter. Here we assume thermionic emission with ohmic contacts for holes, resulting in a high hole density at the contacts [14, 15]. As a consequence, the injection barrier for electrons is approximately equal to the bandgap. The only fit constants to calculate the current are the parameters describing the hole mobility as a function of charge carrier density and temperature.

The undoped P3HT transistor, presented in Fig. 6.1, was numerically simulated using the following mobility parameters: $\sigma_0 = 2.86 \times 10^6\,\mathrm{S/m}$, $T_0 = 350\,\mathrm{K}$, $\alpha^{-1} = 2.6\,\text{Å}$, and $V_{SO} = 2\,\mathrm{V}$. The mobility determined at a gate bias of $-30\,\mathrm{V}$ was $0.03\,\mathrm{cm^2/Vs}$ at room temperature, which is a typical value for P3HT [16, 17]. The solid lines in Fig. 6.1 show that with values rather similar to previously reported numbers [8, 9] a good agreement is obtained. At a certain fixed temperature, arbitrary combinations of σ_0 and α can be found to give identical curves. Therefore, measurements at different temperatures are needed to accurately determine the three parameters. The parameter set is then unique; it not possible to exchange σ_0 and α.

For positive bias, the numerical calculations do predict inversion in the steady-state [18]. However, the calculated electron currents are below the experimental detection limit. The low current is due to the contact definition, the boundary conditions for the contacts strongly influence the calculated current. The highest occupied molecular orbital (HOMO) of P3HT aligns well with the work function of Au, forming an ohmic contact for holes. We assume thermionic emission, resulting in a high hole density at the contacts [14, 15]. As a consequence, the injection barrier for electrons is approximately equal to the bandgap. The corresponding electron density at the contact is very low, leading to low electron currents, even in the presence of an inversion layer. As a result, from undoped semiconductors with ohmic hole contacts it cannot be verified experimentally whether an inversion layer is formed or not.

To address this question we studied the charge transport in deliberately doped semiconductors by using oxidizing agents. By doping the semiconductor as described in Chapter 2, mobile holes are induced yielding a bulk current at zero gate bias. Application of a positive gate bias depletes the semiconductor of holes, to a depth dependent on the gate bias and the doping density [18]. When the depletion depth is larger than the semiconductor layer thickness, the bulk current is completely pinched off. At positive gate bias, when holes are depleted, electrons might be accumulated at the semiconductor-dielectric interface. When such an inversion layer is formed, the accumulated electrons screen the gate potential. A further increase of the gate bias then does not further deplete the bulk semiconductor, but leads to an additional accumulation of electrons. The maximum depletion depth of the semiconductor, $d_{depl,max}$, is given by [18]:

$$d_{depl,max} = \lambda_D \sqrt{4 \ln(N_A/n_i)} \qquad \text{with:} \qquad \lambda_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{sc} k_B T}{e^2 N_A}} \tag{6.1}$$

where λ_D is the Debye length, a characteristic length for charge screening in semiconductors and n_i is the intrinsic carrier density. If the semiconducting layer thickness is larger than the maximum depletion depth, a doped region remains. As a result, also a finite bulk current remains, indirectly indicating the presence of an inversion layer. We note that the screening length is independent of the electron mobility. Hence, even when all electrons are trapped, a finite bulk hole current is expected. In the case that no inversion layer is formed, there are no electrons present to screen the gate bias. An increasing positive gate bias then further depletes the semiconductor and the current is completely pinched off.

We doped the semiconductor in situ by exposing the transistor to a vapor of trichloro(1H,1H,2H,2H-perfluorooctyl)silane (TCFOS), as described in Chapter 2. The doping level in P3HT can be varied deliberately by changing the exposure time [19–21]. The acceptor density ranges between $10^{16}\,\mathrm{cm}^{-3}$ and $10^{17}\,\mathrm{cm}^{-3}$, and n_i is about $1.6 \times 10^4\,\mathrm{cm}^{-3}$, leading to a predicted maximum depletion depth between 40 nm and 200 nm. A semiconductor layer thickness of more than 200 nm was chosen, larger than the predicted maximum depletion depth. Linear transfer curves as a function of exposure time are presented in **Fig. 6.2a**. With increasing exposure time the transfer curves shift towards positive gate bias and a shoulder appears in the sub-threshold region. There is hardly any hysteresis. Gate bias stress can be disregarded on the timescale of the experiment. Each transfer curve represents a single doping level. We stress that for each doping level, the current can be completely pinched off. At high doping levels the semiconductor layer thickness is larger than the predicted maximum depletion depth. The current in depletion being completely pinched off therefore unambiguously shows that no inversion layer is formed. There are no electrons at the semiconductor-dielectric interface to screen the gate potential.

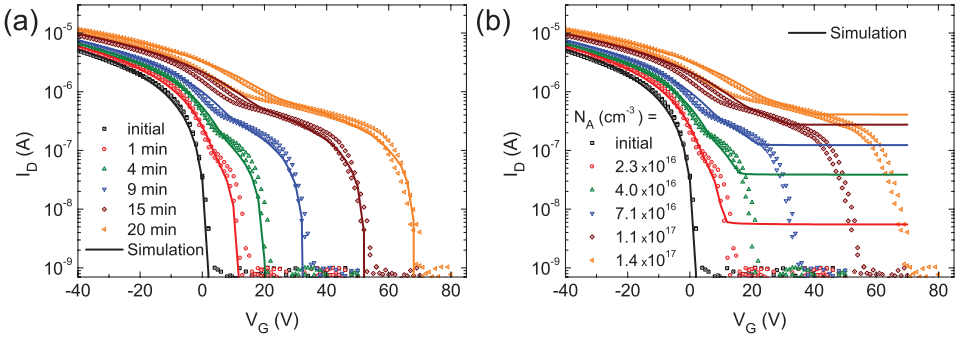

Figure 6.2. Linear transfer curves of a P3HT transistor doped with TCFOS as a function of exposure time, measured at a drain bias of −2 V. The P3HT film thickness was 205 nm and the channel width and length were 2500 µm and 10 µm. (a) Measurements (symbols) and numerical calculations (lines) in which the electron density was artificially suppressed. (b) The same experimental data as in (a). The solid lines are numerical steady-state calculations.

To elucidate the absence of an inversion layer we numerically calculated the transfer characteristics. The doped P3HT transistor in Fig. 6.2 was simulated in several steps. First, the pristine, undoped measurement was described using: $T_0 = 371\,\mathrm{K}$, $\sigma_0 = 1.58 \times 10^7\,\mathrm{S/m}$, $\alpha^{-1} = 1.6\,\text{Å}$, and $V_{SO} = 3\,\mathrm{V}$, slightly different from those of Fig. 6.1. The values are frozen in the calculations of the doped transistors. Upon exposure to the TCFOS a threshold shift is observed. The total threshold shift consists of two distinct voltage shifts: a shift of the switch on voltage, Δ_{SO} and of the pinch-off voltage, V_{pinch}. As described in Chapter 3, from V_{pinch} the acceptor dopant density can be derived, and from Δ_{SO} the interface charge, Q_{if}, can be determined. Next, with the fixed mobility parameters, and a value for N_A and Q_{if}, each doped curve was simulated.

The calculated steady-state currents are presented as solid lines in Fig. 6.2b. In accumulation a good agreement is obtained. In depletion however, a gate independent bulk current is calculated contrary to the experimental currents in Fig. 6.2a. The reason is that in the steady-state an inversion layer is calculated that screens the gate potential and thereby prevents full depletion of the bulk semiconductor. We have calculated the transfer curves by artificially suppressing the electron density in the whole device, as explained in Chapter 3. All other parameters remain the same. The calculated currents are presented as the solid lines in Fig. 6.2a. A good agreement is obtained, which demonstrates that experimentally no inversion layer is formed.

The steady-state densities for holes, electrons and acceptors in the semiconductor are presented in **Fig. 6.3a**, as a function of the distance from the semiconductor-dielectric interface. The densities are calculated in deep depletion. The semiconductor is heavily doped, corresponding to the blue curves in Fig. 6.2. The electron density (red line) is high at the semiconductor-dielectric interface and negligible further down in the semiconductor, forming a clear inversion layer. The hole density (blue line) is negligible at the semiconductor-dielectric interface and reaches further down in the semiconductor the bulk value, forming a depletion region for holes. The depletion width agrees with the calculated maximum depletion width using Eq. 6.1, as indicated by the dashed line in Fig. 6.3a. The net charge in the semiconductor is given by $\rho = e(p - n - N_A)$, and presented in the lower part of Fig. 6.3a. In the bulk there is no net charge, the gate bias is compensated for by the electrons and ionized acceptors in the depletion region. We note that upon increasing the gate bias in steady-state the depletion width does not change. The additional gate bias is fully compensated for by a concomitant increase in accumulated electrons. In Fig. 6.3b, the charge profiles in the semiconductor are presented where the electrons were suppressed. The doping concentration and gate bias are identical to those of Fig. 6.3a. No inversion layer is formed and a larger part of the semiconductor is depleted. The calculated depletion width increases with gate bias. Experimentally there is a large barrier for minority carrier injection. It takes time to form an inversion channel. Hence suppressing the electron density in the calculations corresponds to a transistor that is thermodynamically not in equilibrium. The good agreement between measured and calculated transfer curves indicates that the steady-state is not reached.

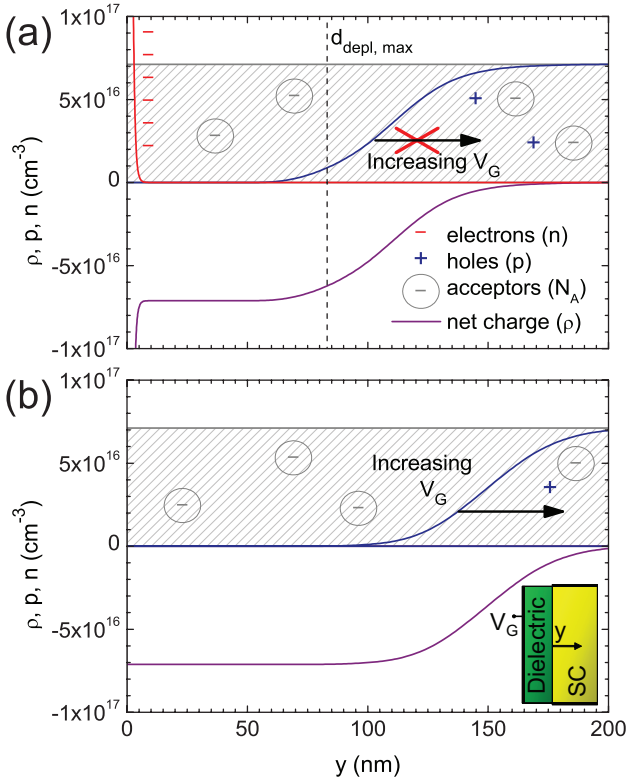

Figure 6.3. Calculated charge density in the semiconductor, plotted versus the distance from the semiconductor-dielectric interface, in the middle of the transistor channel. The acceptor density was $7.1 \times 10^{16}\,\mathrm{cm}^{-3}$. A gate bias of +25 V was applied to deplete the semiconductor from holes. (a) Steady-state calculations. The predicted maximum depletion width is indicated by the dashed line. (b) Electrons are artificially suppressed; the semiconductor is depleted as a function of the gate bias. The y-direction is indicated in the schematic inset.

The minority carriers, here electrons, in the channel can be delivered either by the contacts or by the bulk semiconductor [22]. For standard Si at room temperature the minority carrier response time is determined by generation and is in the order of 0.01–1 s. The fact that silicon transistors operate at GHz frequencies is due to the fact that the minority carriers can be injected from the source and drain regions, which are heavily doped and in close contact to the channel [23]. The generation rate has been estimated for organic semiconductors as a function of the bandgap [23, 24]. The electron generation time in the bulk semiconductor and dielectric relaxation time corresponding to the transport of electrons to the channel, both increase exponentially with the bandgap. The fastest process dominates the dynamic behavior. For a bandgap of 2 eV a response time of more than 10^6 s has been calculated [23]. Hence the supply of electrons from the bulk semiconductor can be disregarded.

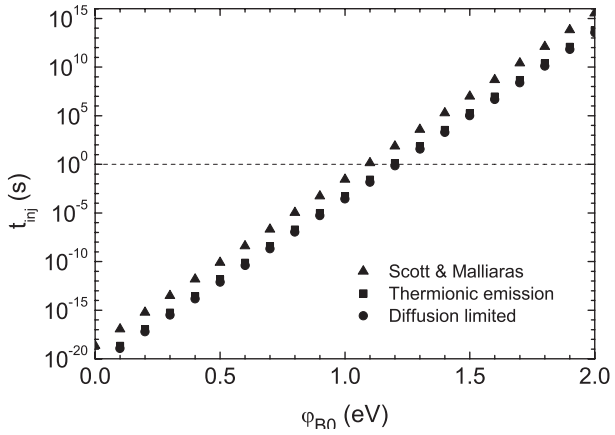

Figure 6.4. The time required to inject the steady-state charge in a field-effect transistor, calculated using three injection models. The calculations are based on a transistor with a width, length, and height of 2500 µm, 10 µm, and 205 nm and a gate bias of 10 V. The value for the Richardson constant was estimated as $100\,\mathrm{AK^{-2}cm^{-2}}$ (Si), the mobility was $0.01\,\mathrm{cm^2/Vs}$, the electric field at the injecting contact was $5 \times 10^6\,\mathrm{V/cm}$, and the density of states of the valence band was $2 \times 10^{21}\,\mathrm{cm^{-3}}$. The dashed line indicates the time scale of the measurement.

In order to form an inversion layer, the carriers have to be supplied by the electrodes. The injection time is estimated from the total accumulated charge density and the injection current that can be delivered by the contact. The accumulation charge is approximated by $V_G C_i$, resulting in $10^{12}\,\mathrm{electrons/cm^2}$ at a typical gate bias of 10 V. For a transistor with a width and length of 2500 µm and 10 µm, the charge to be injected amounts to $4.3 \times 10^{-11}\,\mathrm{C}$. We calculate the injection current as a function of injection barrier, which is the difference in work function of the electrode and the lowest unoccupied molecular orbital (LUMO) energy of the semiconductor. We take as injection mechanism thermionic emission with image-force lowering of the barrier, and two reported diffusion limited injection models [18, 25]. The calculated injection times as a function of injection barrier are presented in **Fig. 6.4**. The injected current and hence the injection time depend exponentially on the injection barrier. Therefore in Fig. 6.4 straight lines are obtained. The injection barrier for P3HT and Au is about 1.7 eV. Figure 6.4 shows that the injection time is at least 10^8 s. This value is much larger than realistic measurement times, showing that the transistor is not in thermodynamic equilibrium. We note that in ambipolair transistors, which conduct both electrons and holes, the injection barriers are typically 1 eV or less. The calculated equilibrium times are less than 1 s, which confirms that both electrons and holes can indeed be supplied by the contacts within the experimental measurement time. Similarly it should be noted that when electron injecting source-drain contacts such as Ca or Ba are applied, the inversion layer will be formed in the time frame of the experiments, in agreement

with the observations of Chua et al. [7]. In that case the barrier for hole injection will be large, such that the formation of the hole accumulation layer at negative gate bias will be strongly hampered.

6.3 Summary

We have investigated the formation of an inversion layer in organic normally-ON unipolar *p*-type transistors. At positive gate bias the measured current is negligible. The absence of the electron current can be due to trapping or to limited electron injection. By studying the depletion current of unipolar *p*-type transistors based on a deliberately doped organic semiconductor we can disentangle these mechanisms since an inversion layer screens the gate bias. Numerically calculated steady-state currents show in accumulation a good agreement with experimental currents. In depletion agreement could only be obtained by suppressing the electron density, which demonstrates that experimentally no inversion layer is formed. In order to form an inversion layer, the carriers have to be supplied by the electrodes. We estimate the injection time assuming thermionic emission or diffusion limited injection models as the injection mechanism. For a barrier of 1.7 eV we arrive at an injection time of at least 10^8 s. Hence an inversion layer is not formed because the transistors are not in thermodynamic equilibrium.

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Charge transport in dual-gate organic field-effect transistors

7

Abstract

The charge carrier distribution in dual-gate field-effect transistors is investigated as a function of semiconductor thickness. A good agreement with two-dimensional numerically calculated transfer curves is obtained. For semiconductor thicknesses larger than the accumulation layer thickness, two spatially separated channels are formed. The cross-over from accumulation to depletion of the two channels in combination with a carrier-density dependent mobility causes a shoulder in the transfer characteristics. A semiconducting monolayer transistor has only a single channel. The charge carrier density, and consequently the mobility, are virtually constant and change monotonically with applied gate biases, leading to transfer curves without a shoulder.

7.1 Introduction

Most organic transistors are unipolar *p*-type, they can only support holes. The threshold voltage is typically slightly positive yielding normally-ON devices. Therefore, integrated circuits are based on zero-V_{GS}-load topology, whereby the gate of the load transistor is connected to its source. This topology suffers from an inherently small noise margin, which is a measure for the maximum allowed spurious signal that can be accepted by the gate while still giving the correct operation. The noise margin can dramatically be improved by using dual-gate transistors to set the threshold voltage [1]. The layout of a dual-gate transistor contains an additional gate dielectric and electrode [2, 3]. The second gate electrode modifies the charge carrier distribution in the channel accumulated by the first gate. As introduced in Chapter 1, the shift in the threshold voltage for the bottom gate is given by [4–7]:

$$\Delta V_{t,bot} = -\frac{C_{top}}{C_{bot}} \Delta V_{top} \tag{7.1}$$

where C_{top} and C_{bot} are the capacitances per unit area of the top and bottom dielectric, and V_{top} is the top gate bias. The largest reported integrated circuit is based on dual-gate transistors [8]. The increased noise margins more than justifies the additional process steps.

The charge transport in dual-gate transistors is not yet fully understood. The transfer curves often show a typical 'shoulder': in depletion the transconductance does not monotonically decrease with increasing gate bias. This anomaly has been ascribed to the capacitance of the semiconductor [6]. To investigate the charge transport and the origin of the anomaly we fabricated dual-gate transistors where we deliberately varied the semiconductor layer thickness.

The current depends on the charge carrier density and the mobility. Both the top and bottom gates determine electrostatically the charge carrier density. A complication arises because for organic semiconductors the mobility itself depends on the charge carrier density. As a result, the common one-dimensional (1D) approximations for the carrier distribution [9, 10] cannot be used to describe the charge profile of the two interacting channels in a dual-gate transistor. Therefore, a 2D analysis is required. The transfer curves were modeled numerically using the 2D device simulator CURRY [11–13]. We have fabricated dual-gate transistors with varying semiconductor layer thickness. The electrical transport has been measured as a function of biases, and transfer curves have been simulated numerically. We show that the shoulder presented by the transfer characteristics is due to the charge distribution in combination with a charge carrier density dependent field-effect mobility.

7.2 Results and discussion

Dual-gate transistors were fabricated as explained in detail in Chapter 2. To minimize the influence of short-channel effects and contact resistances, channel lengths larger than 10 µm were used. As a semiconductor poly(2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene) (MEH-PPV) with a thickness of 40 nm was used. Alternatively, self-assembled monolayer field-effect transistors (SAMFET) of chloro(11-(5""-ethyl- 2,2:5',2":5",2"':5"',2""-quinquethien-5-yl)undecyl) dimethylsilane were fabricated [14]. As top gate dielectric, poly(methyl methacrylate) (PMMA) and poly(isobutyl methacrylate) (PIBMA) were applied, respectively, with a thickness of 300 nm and 600 nm. The devices were finished by evaporation of a Ag or Au top gate electrode. To calculate the current in the dual-gate transistors, 2D numerical simulations were performed, as described in Chapter 3. Electrical conduction in organic semiconductors occurs by thermally activated hopping of charge carriers between localized states. We included variable range hopping by implementing the mobility as described in Chapter 1, according to Eq. 1.2 [15]. The boundary conditions were ohmic contacts for holes and blocking contacts for electrons [16, 17].

Linear transfer curves of a dual-gate transistor with a 40 nm thick MEH-PPV semiconductor are presented in **Fig. 7.1**. The top gate is swept at fixed bottom gate biases in Fig. 7.1a, while in Fig. 7.1b the bottom gate is swept at fixed top gate biases. The transfer curves shift with applied fixed gate biases. Figure 7.1c shows that the shift in threshold voltage depends on the capacitive coupling as given by Eq. 7.1. The shoulder in the transfer curves shown in Fig. 7.1a (Fig. 7.1b) gets more pronounced at more negative bottom (top) gate biases. For a semiconductor layer of 40 nm thick, the corresponding depletion capacitance is larger than the top and bottom gate capacitances and, therefore, cannot be the origin of the shoulder.

To elucidate the origin we numerically modeled the transport. The semiconductor thickness of 40 nm is an order of magnitude larger than the thickness of the accumulation layer, estimated to be about 2 nm [10]. Therefore, we can describe the dual-gate transistor with a spatially separated top and bottom channel. The channels have chemically dissimilar interfaces. Due to the corresponding differences in e.g. interface roughness [3, 4] and dipolar disorder [18] the transport parameters are not identical, and have to be determined separately. We take a top gate bias at the threshold voltage, here about 0 V. The source-drain current is then dominated by the bottom channel. By fitting the calculated current to the experimental data the transport parameters for the bottom channel can be determined. A similar procedure holds for the top channel. In the simulations, we divide the film in half and assign the top and bottom transport parameters accordingly. The current is then calculated for all other combination of gate biases and presented as the solid lines in Fig. 7.1, resulting in a good agreement.

Parameters extracted for the bottom channel are $T_0 = 510\,\mathrm{K}$, $\sigma_0 = 8.65 \times 10^6\,\mathrm{S/m}$, $\alpha^{-1} = 1.4\,\text{Å}$, and for the top channel $T_0 = 400\,\mathrm{K}$, $\sigma_0 = 1.43 \times 10^5\,\mathrm{S/m}$, $\alpha^{-1} = 1.4\,\text{Å}$. The parameter values are comparable to those reported previously [10]. We note that the main difference is that the mobility in the top channel is effectively a factor of five lower than that of the bottom channel. The difference can be due to differences in interface roughness and or morphology. The threshold voltages of the bottom and top channel are +10 V and 0 V. These values are mainly related to fixed interface charges, implemented in the numerical simulation as a layer of fixed charges at the bottom dielectric interface, Q_{if}.

As is shown in Fig. 7.1, the shoulder appears at biases where one channel is in accumulation, and the other channel switches from accumulation to depletion. The origin is elucidated in Fig. 7.1d. Going from negative to positive bottom bias, first the bottom channel is depleted followed by depletion of the fixed top channel. Since the average charge carrier density in the two channels is different and because

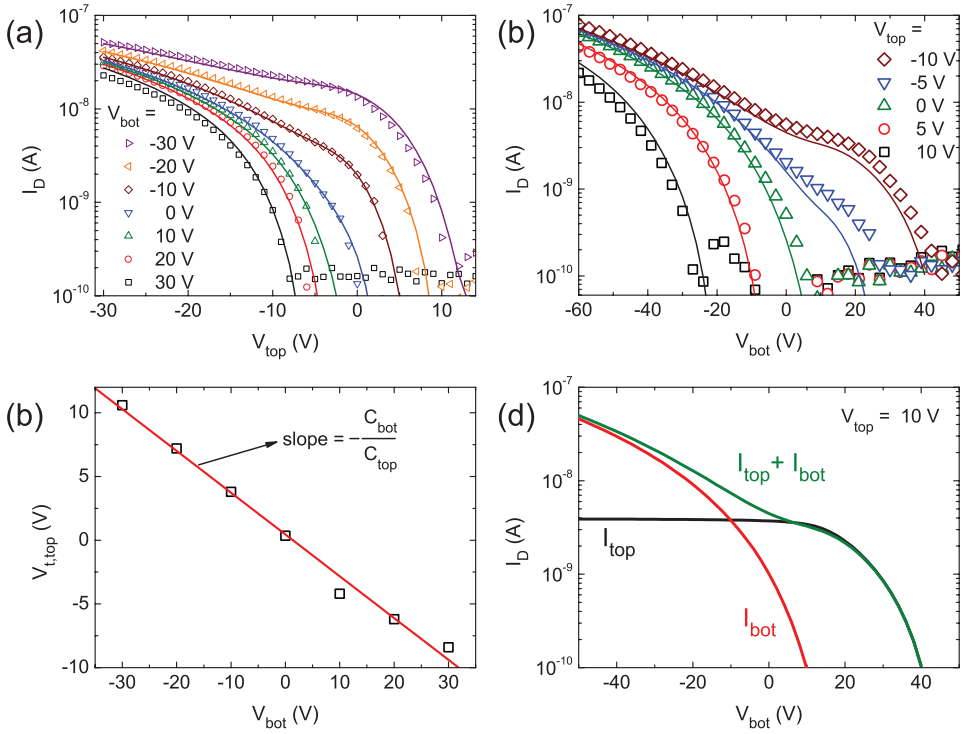

Figure 7.1. Linear transfer curves of a dual-gate transistor with a 40 nm thick semiconducting MEH-PPV layer. Measurements are presented as symbols and numerical calculations as solid lines. The drain bias was 5 V and the channel width and length were 20 000 µm and 20 µm. (a) Top gate scans at fixed bottom gate biases and (b) bottom gate scans at fixed top gate biases. (c) Top threshold voltage as a function of the bottom bias. (d) Calculated total current and the separate currents flowing in the top and bottom channel, for $V_{top} = 10$ V.

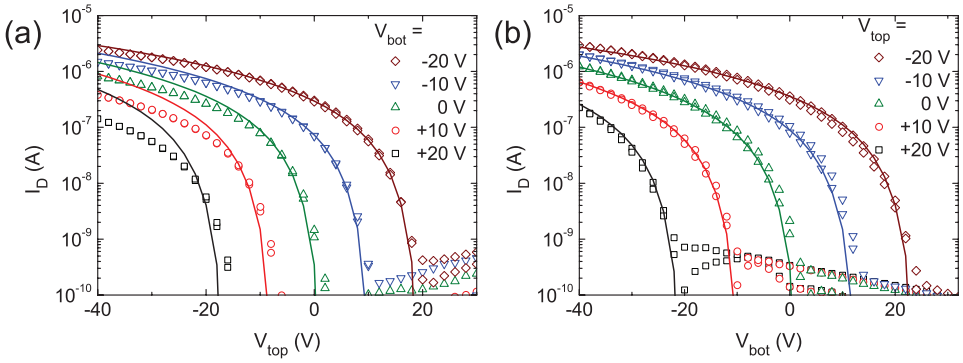

Figure 7.2. Linear transfer curves of a dual-gate SAMFET. Measurements are presented as symbols and numerical calculations as solid lines. The drain bias was 2 V and the channel width and length were 10 000 µm and 10 µm. (a) Top gate scans at fixed bottom gate biases and (b) bottom gate scans at fixed top gate biases.

the mobility is charge carrier dependent, the drain current superlinearly decreases with increasing bottom gate bias. The carrier dependent mobility therefore leads to a different effective mobility in each channel, yielding a shoulder in the transfer curve.

To confirm that a shoulder is due to spatially different key transport parameters a transistor would be required of which the layer thickness is comparable to the accumulation thickness. In that case only a single homogeneous channel is expected. For this purpose we fabricated a dual-gate SAMFET of which the active channel is only one monolayer thick. The transfer curves of the dual-gate SAMFET are presented in **Fig. 7.2**. The top gate is swept at fixed bottom gate biases in Fig. 7.2a, while in Fig. 7.2b the bottom gate is swept at fixed top gate biases. The transfer curves shift with applied fixed gate bias in agreement with the capacitive coupling. The solid lines in Fig. 7.2 are now calculated using a single parameter set for the mobility function ($T_0 = 600\,\mathrm{K}$, $\sigma_0 = 1.45 \times 10^9\,\mathrm{S/m}$, $\alpha^{-1} = 1.6\,\text{Å}$). A good agreement is obtained. The small deviations in accumulation (see Fig. 7.2a) might be due to a limited injection caused by under-etched electrodes [14]. For the SAMFET, the source-drain current is a monotonic function of the gate biases. No shoulder is observed while the mobility still depends on the carrier density.

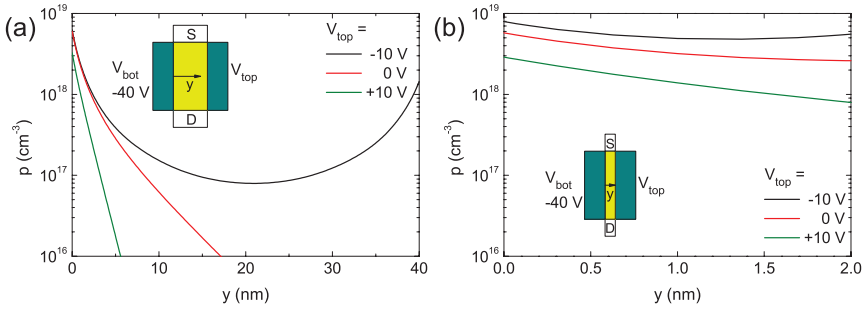

Figure 7.3. Calculated hole density in a dual-gate transistor as a function of position in the semiconductor between both gate dielectrics. The inset shows the transistor layout schematically and indicates the y-direction. A negative bottom gate bias is applied and the top gate bias is varied. The semiconductor thickness was (a) 40 nm and (b) 2 nm.

Calculated carrier profiles, $p(y)$, for the dual-gate MEH-PPV transistor and the SAMFET are presented in **Fig. 7.3a and b** respectively. The bottom gate is always in accumulation. The top gate is either in accumulation (black lines), grounded (red lines) or in depletion (green lines). With both gates in accumulation, the hole density in the 40 nm thick MEH-PPV semiconductor varies over two orders of magnitude between both gates. Figure 7.3a shows that two spatially separated channels are formed. Due to its carrier density dependence, the conductivity varies over more than two orders of magnitude. This clearly explains why the switch of one channel from depletion to accumulation gives rise to a strong increase of the current, which results in the shoulder shown in Fig. 7.1. For the grounded and depleted cases, the density variation is even larger. Figure 7.3b shows that the carrier concentration in the SAMFET is within one order of magnitude for all biases. The charge carrier concentration in the dual-gate SAMFET is virtually constant. Only a single transport channel is formed. Hence a transition from one to two channels cannot occur and a shoulder in the transfer characteristics is absent. Whether a shoulder appears in the transfer characteristics or not, depends on the semiconductor thickness, both channel mobilities, and whether the mobilities are constant or carrier-density dependent. An overview is given in Table 7.1.

Channel mobility	Shoulder? semiconductor thickness > 10 nm	< 10 nm
$\mu_{top} = \mu_{bot}$, constant	N*	N
$\mu_{top} \neq \mu_{bot}$, constant	Y	N
$\mu_{top} = \mu_{bot}$, density dependent	Y	N
$\mu_{top} \neq \mu_{bot}$, density dependent	Y	N

Table 7.1. Whether a shoulder appears in the transfer characteristics or not, depends on both channel mobilities and whether the mobilities are constant or charge-carrier-density dependent. *Provided the semiconductor capacitance is much larger than the gate capacitances.

7.3 Summary

The charge carrier distribution in organic dual-gate field-effect transistors has been investigated using 2D numerical simulations. A carrier density dependent mobility based on variable range hopping has been implemented. A good agreement with experimental transfer curves has been obtained. When the layer thickness is much larger than the accumulation width, two spatially separated channels are formed. The cross-over from accumulation into depletion of the two channels in combination with a different effective mobility causes a distinct shoulder in the transfer characteristics. In a dual-gate SAMFET the thickness of the semiconductor is equal to that of the accumulation layer, hence there is only one channel. The charge carrier density, and consequently the mobility, is virtually constant throughout the semiconductor and they change monotonically with applied gate biases, leading to transfer curves without a shoulder.

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Two-dimensional charge transport in disordered organic semiconductors

8

Abstract

In Chapter 7 the semiconducting monolayer transistor was introduced in a dual-gate structure. In this Chapter, we analyze the effect of carrier confinement on the charge transport properties of organic field-effect transistors in more detail. Confinement is achieved experimentally by the use of semiconductors of which the active layer is only one molecule thick. The two-dimensional confinement of charge carriers provides access to a previously unexplored charge-transport regime, and is reflected by a reduced temperature dependence of the transfer curves of organic monolayer transistors.

8.1 Introduction

The availability of semiconducting materials of unprecedented purity and crystalline perfection has enabled the realization of semiconductor nanostructures. Devices have been fabricated that contain a thin layer of highly mobile electrons. The motion perpendicular to the layer is inhibited; the electrons are constrained to move laterally in a plane, forming a two-dimensional electron gas (2DEG). Electronic properties of the 2DEG in Si metal-oxide-semiconductor field-effect transistors (MOSFETs) have been reviewed by Ando, Fowler, and Stern [1]. By application of a sufficiently strong positive voltage V_G on the gate, a 2DEG is induced electrostatically in the p-type Si just under the SiO_2 gate dielectric. Due to the large electric field at the Si-SiO_2 interface an approximately triangular potential well is formed. The confinement in the potential well causes the three-dimensional (3D) conduction band to split into a series of two-dimensional subbands. Alternatively, in a modulation-doped GaAs-$Al_xGa_{1-x}As$ heterostructure, the 2DEG is formed in GaAs at the interface with the $Al_xGa_{1-x}As$ layer [2]. Here, the electrons are confined to the GaAs-$Al_xGa_{1-x}As$ interface by a potential well formed by the repulsive barrier due to the conduction band offset between the two semiconductors. The electrons in the GaAs 2DEG originate from donors in the $Al_xGa_{1-x}As$ layer that are spatially separated from the interface by an undoped AlGaAs spacer layer to reduce scattering. Again, two-dimensional subbands are formed as a result of confinement perpendicular to the interface, but now the 2DEG is present 'naturally' due to the modulation doping without the requirement of a gate bias. Because of the absence of boundary scattering at the interface, the electron mobility can be higher by many orders of magnitude as compared to bulk values.

A 2DEG offers the possibility to study quantum transport in macroscopic systems, due to the combination of a large Fermi wavelength (40 nm) and large mean free path (exceeding 10 µm). Two-dimensional systems in a perpendicular magnetic field have the remarkable property of a quantized Hall resistance [3] which results from the quantization of the 2D subbands in a series of Landau levels. The ultimate 2D confinement of charge carriers in a single atomic layer occurs in graphene, a molecular sheet of carbon atoms in a honeycomb crystal lattice. Due to the fact that charge carriers in graphene act as massless relativistic particles with only very limited scattering, the quantum hall effect can be observed even at room temperature [4].

In the last decades organic semiconductors, π-conjugated polymers and small molecules, have been studied intensively. The charge transport occurs by hopping, which is phonon-assisted tunneling, between disorder-induced localized states at the Fermi level. The density of localized states (DOS) can be described by a Gaussian [5] or an exponential [6] distribution. With increasing carrier density, the tail states of the DOS get filled. The charge carriers have more transport states available at higher energy and, therefore, the average mobility increases. For bulk conduction, a transport model has been derived based on variable range hopping and percolation by Vissenberg and Matters (V-M), as presented in Chapter 3 [6]. This model gives an analytical description for the bulk conductivity as a function of carrier density and temperature. The hopping distance, which reflects the mean

free path of a carrier in a disordered organic semiconductor, is typically 1–10 nm, depending on the carrier density.

Similar to charge carriers in Si-based MOSFETs, carriers in organic semiconductors can also be confined in a field-effect transistor (OFET) at the semiconductor-dielectric interface [7]. The dependence of the measured field-effect mobility on semiconductor thickness has been reported for a number of organic compounds. For semiconductors deposited by vacuum sublimation the determined mobility typically saturates after 2–6 monolayers [8–10] depending on the growth mode [10]. The fact that charge transport is observed even in a single organic monolayer [8] has opened the possibility of using a semiconducting self-assembled monolayer as active component in an OFET. In a self-assembled monolayer field-effect transistor (SAMFET) the semiconductor is a single molecular layer formed spontaneously on the gate dielectric. Recently the first SAMFETs were reported and combined into integrated circuits [11]. The demonstration of logic functionality makes self-assembly the ultimate technology for bottom-up mass production of organic electronics [12–15]. In a SAMFET, the semiconductor layer thickness is comparable to that of the accumulation layer, i.e. 2 nm, as studied in detail in Chapter 7. The electrical transport is then by definition two-dimensional. However, the reported charge carrier mobilities in SAMFETs are similar to the corresponding bulk mobilities. In spite of the strong confinement within the single sheet of molecules, no special signatures of 2D charge transport have been observed in SAMFETs. The fundamental question is now whether 2D transport or confinement effects play a role in organic transistors. Intuitively, one could argue that because of the small mean free path of the charge carriers, typically equal or slightly larger than the thickness of a monolayer, these effects will be small or absent. In this Chapter, we investigate the charge transport in monolayer OFETs and show that 2D carrier confinement is reflected in the transfer characteristics. We demonstrate that the 2D confinement of charge carriers leads to a reduced temperature dependence of the transfer curves.

8.2 Results and discussion

An OFET typically operates in accumulation mode, where the charges are electrostatically confined in the first few nanometers of the semiconductor near the dielectric interface [16]. The majority of the semiconductor is depleted and acts as an insulator. The current was calculated using the V-M model [6] and an accurate description of the transport in an OFET as a function of temperature and gate bias has been demonstrated. The transport is characterized by a power-law relationship between the conductivity and the carrier concentration at the semiconductor-dielectric interface, due to the filling of the tail of the DOS. The power-law exponent is determined by the shape of the exponential DOS. In this Chapter, we focus again on p-type OFETs, where holes are mainly responsible for the conduction. In the V-M model the conductivity has been derived as a function of the carrier density and temperature, as described by Eq. 1.2.

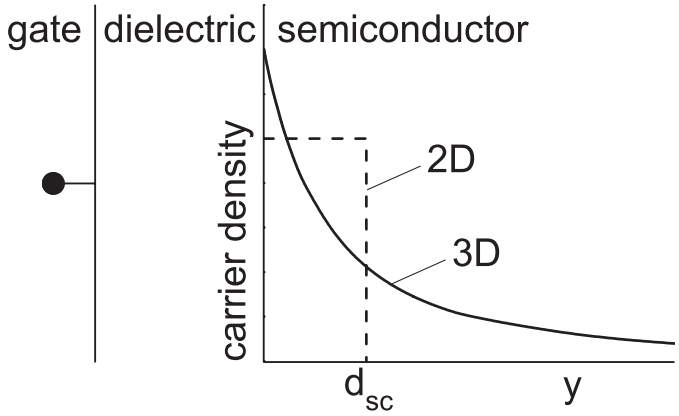

Figure 8.1. Charge carrier density as a function of distance from the semiconductor-gate dielectric interface, y, in an organic field-effect transistor (OFET). In a semi-infinitely thick semiconductor the charges distribute in 3D, resulting in a density that decreases with the square of the distance from the interface. In a monolayer semiconductor with a thickness d_{sc}, the carriers are confined in 2D, and a constant carrier density is expected.

Spin-coated film as semiconductor

To calculated the current, an expression for the hole density is required. For an semi-infinitely thick semiconductor with an exponential DOS, the hole density in the accumulation layer decreases quadratically with the distance from semiconductor-dielectric interface, as described by Eq. 3.8. The hole distribution perpendicular to the semiconductor-dielectric interface is illustrated in **Fig. 8.1**. In the linear regime, when the drain bias, V_D, is much smaller than the gate bias, V_G, the potential in the channel gradually changes between source and drain. The source-drain current can be derived by integrating the sheet conductance $G_{sh}(V_x) = \int_0^{d_{SC}} ep\mu_p(p)\,dy$ over the potential between the source and drain, where V_x is difference between the gate bias and the local channel potential at a point x in the channel. When using the hole distribution of Eq. 3.8, the hole current for $|V_G - V_t| \geqslant |V_D|$ reads [17]:

$$\begin{aligned} {I_D}^{3D} &= f\frac{W}{L}\left(\frac{1}{2k_BT_0\varepsilon_0\varepsilon_{sc}}\right)^{\frac{T_0}{T}-1} {C_i}^{\frac{2T_0}{T}-1}\frac{T}{2T_0}\frac{T}{2T_0-T} \\ &\quad\times\left(\|V_{SO}-V_G\|^{\frac{2T_0}{T}} - \|V_{SO}-V_G+\ V_D\,\|^{\frac{2T_0}{T}}\right) \end{aligned} \tag{8.1}$$

with f is a temperature, T, dependent prefactor given by:

$$f = \frac{\sigma_0}{e}\left[\frac{\left(\frac{T_0}{T}\right)^4 \sin\left(\frac{\pi T}{T_0}\right)}{(2\alpha)^3 B_C}\right]^{\frac{T_0}{T}}$$

where σ_0 is a conductivity prefactor, T_0 is a characteristic parameter describing the width of the exponential DOS, and α^{-1} is an effective overlap parameter. The channel width and length are denoted by W and L, and V_{SO} is the switch-on voltage, defined as the gate bias at the onset of accumulation. The remaining parameters have their usual meaning. Equation 8.1 was already introduced in Chapter 3, but is presented once more for clarity. By using the Taylor expansion $(1-r)^\kappa \approx 1 - \kappa r + \ldots$ for small $r = V_D/(V_{SO} - V_G)$, the current I_D at high gate bias can be approximated by:

$${I_\mathrm{D}}^{\mathrm{3D}} \propto (V_{SO} - V_G)^{\frac{2T_0}{T}-1} \tag{8.2}$$

The validity of this model can easily be exemplified by studying the charge transport in organic transistors where charge carriers can distribute in 3D. As a model compound we used spin-coated films of poly(3-hexylthiophene) (P3HT). Au source and drain contacts form an ohmic contact for holes, yielding unipolar *p*-type P3HT transistors. The transistors were fabricated as described in Chapter 2. We note that the film thickness was larger than 80 nm, much thicker than the hole accumulation layer. Transfer curves were measured as a function of temperature at low drain bias and are presented in **Fig. 8.2a**. The current increases with increasing negative gate bias and with increasing temperature. As expected from Eq. 8.2, at high gate bias a power-law dependence of the current on the gate bias is observed, as presented on a double logarithmic scale in Fig. 8.2b. For each temperature, the exponent of the observed power law was plotted versus $1/T$. A straight line was found, as shown in Fig. 8.2e. The extrapolated line crosses the exponent axis at the value of -1, as predicted by Eq. 8.2 for $T \to \infty$. This agreement indicates indirectly that the charge carrier profile calculated for an infinite semiconductor thickness is indeed valid for the P3HT transistor. We performed similar analysis on literature data of OFETs based on poly(2,5-thienylene vinylene) (PTV) and poly(2-methoxy-5-(3',7'-dimethyloctyloxy)-p-phenylene vinylene) (MDMO-PPV) [18, 19]. In both cases a power-law dependence was observed. The extrapolated exponents cross at -1 in a $1/T$ plot, as shown in Fig. 8.2e. From the slopes of Fig. 8.2e the values for T_0 can be found, the parameter that indicates the width of the exponential DOS. For P3HT, MDMO-PPV and PTV we obtain $T_0 = 402$ K, $T_0 = 500$ K, and $T_0 = 441$ K, respectively. Using the determined T_0, the transfer curves as a function of bias and temperature can be fully described using Eq. 8.1, as presented by the solid lines in Fig. 8.2a for P3HT. The calculations for MDMO-PPV and PTV are presented in (c) and (d) of the same Figure.

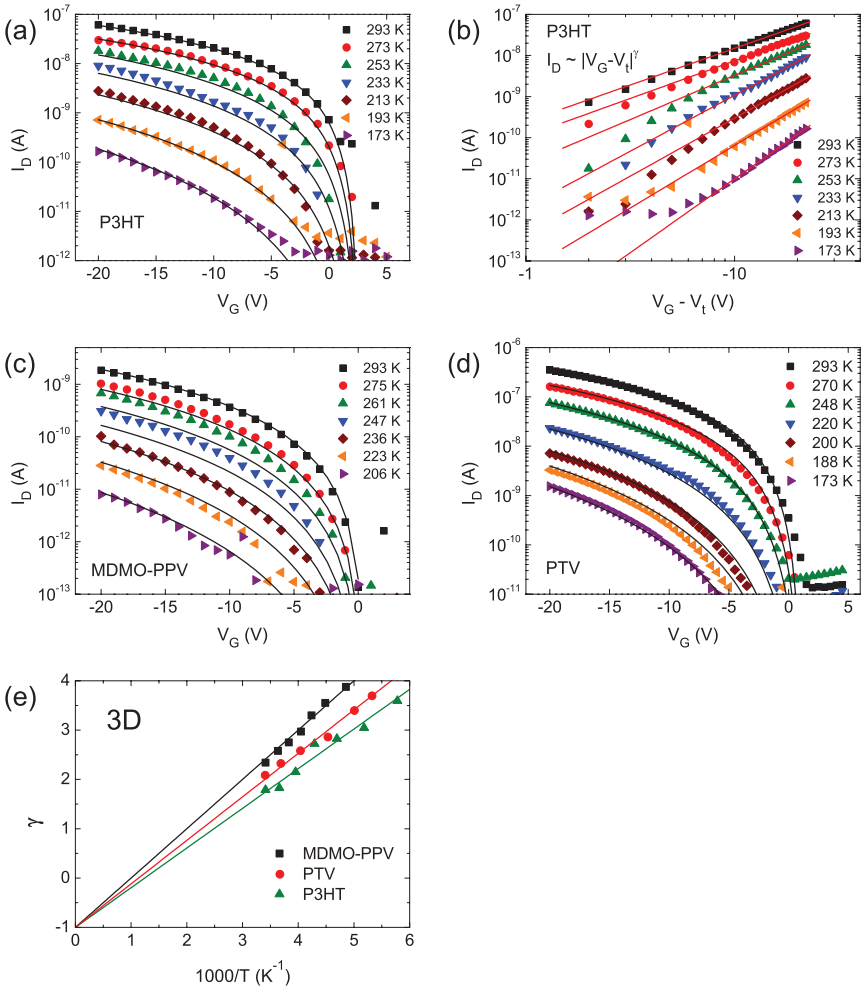

Figure 8.2. 2 (a, c, d) Experimental transfer curves of spin-coated thin-film transistors, measured as a function of temperature. The semiconductor was a film of (a) P3HT, (c) MDMO-PPV, and (d) PTV. The drain bias was $-2\,\mathrm{V}$ (P3HT and PTV), or $-0.1\,\mathrm{V}$ (MDMO-PPV). The current was described using Eq. 8.1, presented as black lines, using the following parameters: For P3HT: $T_0 = 402\,\mathrm{K}$, $\sigma_0 = 1.76 \times 10^6\,\mathrm{S/m}$, $\alpha^{-1} = 1.4\,\text{Å}$, $V_{SO} = 2.5\,\mathrm{V}$, and $W/L = 2500\,\mu\mathrm{m}/10\,\mu\mathrm{m}$. The semiconductor thickness was 80 nm. For MDMO-PPV: $T_0 = 500\,\mathrm{K}$, $\sigma_0 = 1.1 \times 10^8\,\mathrm{S/m}$, $\alpha^{-1} = 0.91\,\text{Å}$, $V_{SO} = 0.5\,\mathrm{V}$, and $W/L = 2500\,\mu\mathrm{m}/10\,\mu\mathrm{m}$. For PTV: $T_0 = 441\,\mathrm{K}$, $\sigma_0 = 1.8 \times 10^6\,\mathrm{S/m}$, $\alpha^{-1} = 1.9\,\text{Å}$, $V_{SO} = 1\,\mathrm{V}$, and $W/L = 20\,\mathrm{mm}/20\,\mu\mathrm{m}$. (b) The experimental P3HT data (Fig. 8.2a) plotted on a double logarithmic scale, corrected for a threshold voltage of 2.5 V. The red lines are a power-law fit at high gate bias, for each temperature. (e) The power-law exponent γ extracted from Fig. 8.2b versus $1/T$. A similar analysis was performed on the MDMO-PPV and PTV data [18, 19]. The solid lines are a guide to the eye.

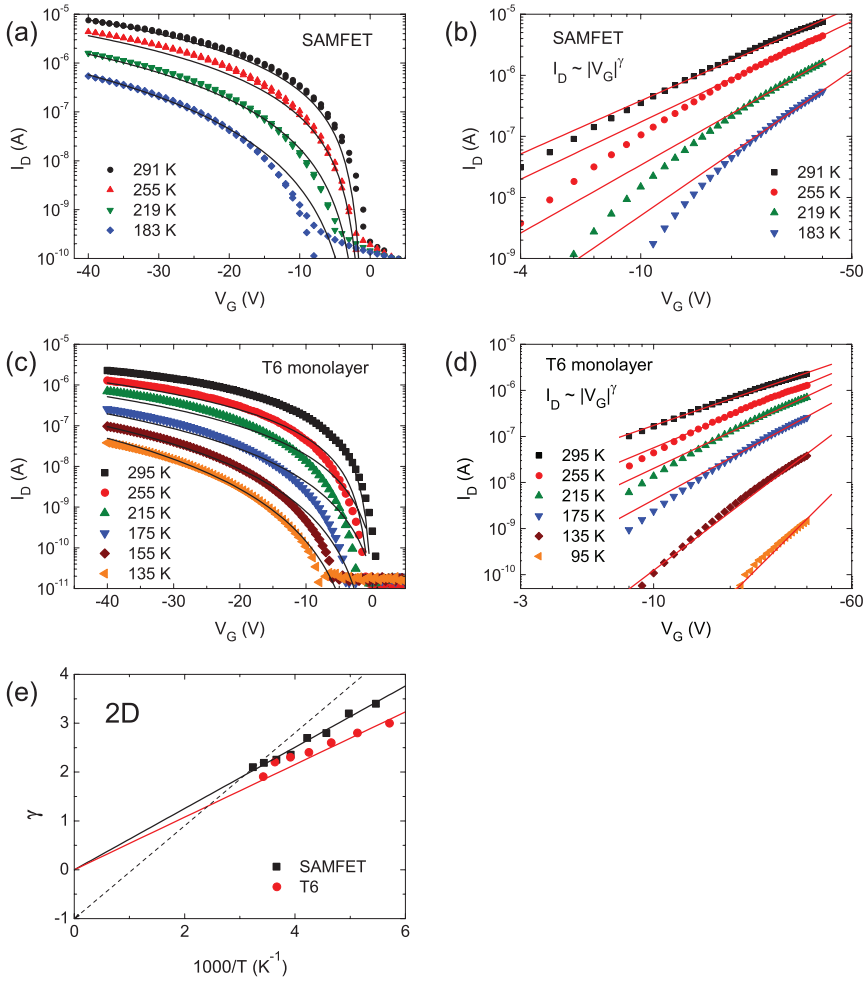

Figure 8.3. (a, c) Experimental transfer curves measured as a function of temperature, at a drain bias of $V_D = -2$ V, of a (a) SAMFET, and (b) T6 monolayer transistor. The currents calculated according to Eq. 8.4, based on a step-function carrier distribution, are presented as black lines. The used parameters were: For the SAMFET: $T_0 = 627\,\mathrm{K}$, $\sigma_0 = 4 \times 10^6\,\mathrm{S/m}$, $\alpha^{-1} = 4.3\,\text{Å}$, $V_{SO} = -1\,\mathrm{V}$, and $W/L = 20\,000\,\mu\mathrm{m}/20\,\mu\mathrm{m}$. For the T6 monolayer transistor: $T_0 = 539\,\mathrm{K}$, $\sigma_0 = 7.5 \times 10^5\,\mathrm{S/m}$, $\alpha^{-1} = 4.5\,\text{Å}$, $V_{SO} = 0 - 3$ V, and $W/L = 2500\,\mu\mathrm{m}/10\,\mu\mathrm{m}$. The semiconductor thickness was taken as 2 nm. (b, d) The same experimental data as in Fig. 8.3a and 8.3c plotted on a double logarithmic scale. The red lines are a power-law fit at high gate bias, for each temperature. (e) The exponent extracted from Fig. 8.3b and 8.3d versus inverse temperature. The solid lines are a guide to the eye. Extrapolating the monolayer data to infinite temperature does not agree with Eq. 8.2, as indicated by the dashed line.

Monolayer semiconductor

To study the charge transport in a transistor where charges are physically confined to a 2D semiconducting monolayer, we fabricated SAMFETs and transistors with an evaporated monolayer, as described in detail in Chapter 2. The SAMFETs were fabricated by self-assembly of a monolayer of the conjugated molecule chloro(11-(5""-ethyl-2,2:5',2":5",2"':5"',2""-quinquethien-5-yl)undecyl) dimethylsilane between the source and drain electrodes. The evaporated monolayer transistors were fabricated from α-sexithiophene (T6). In both cases, ohmic contacts for holes are formed with Au, yielding p-type transistors.

Linear transfer curves of a SAMFET were measured as a function of temperature and are presented in **Fig. 8.3a**. Transfer curves of a T6 monolayer transistor are plotted in Fig. 8.3c. Similar to the transistors with a thick semiconductor, the current decreases for lower temperatures. Furthermore, a power-law dependence of the current on gate bias is observed at high gate bias, see Fig. 8.3b and 8.3d. The extracted exponent of the power law for each curve is plotted versus inverse temperature in Fig. 8.3e. Again a straight line was found. However, the extrapolated line does not cross the exponent axis at a value of -1, but at a value close to 0. The temperature dependence of the power-law exponent of the SAMFETs and T6 monolayer transistors is weaker than that for the thick semiconductors.

The question is whether the weaker temperature dependence in the monolayer transistors is related to the carrier distribution. To answer this question, we compare the carrier distribution in thick and thin semiconducting films, and we study the impact of the distribution on the charge transport. As shown above, in a thick semiconductor, the carrier density decreases with the square of the distance from the semiconductor-gate dielectric interface. However, for a monolayer semiconductor, the assumption of infinite thickness does not hold. The carriers accumulated by the gate bias are confined in the monolayer; there is no space to redistribute. Therefore, a density proportional to the gate bias, but uniform in the semiconductor seems reasonable, as illustrated by the step-function in Fig. 8.1. The local hole density then reads:

$$p = \frac{C_i V_x}{e d_{sc}} \tag{8.3}$$

where d_{sc} is the semiconductor thickness. As the semiconductor thickness we take 2 nm, the length of the conjugated part of the molecule. Using this step-function carrier profile, an expression for the current can be derived.

We start with the Vissenberg-Matters mobility of Eq. 1.2. The source-drain current can again be derived by integrating the sheet conductance $G_{sh}(V_x) = \int_0^{d_{SC}} ep\mu_p(p)\,dy$ over the potential between the source and drain. However, now we use the step-function for the hole concentration of Eq. 8.3. The current then reads:

$$\begin{aligned} {I_D}^{\mathrm{2D}} &= f\frac{W}{L}(ed_{sc})^{1-\frac{T_0}{T}}(C_i)^{\frac{T_0}{T}}\frac{T}{T_0+T} \\ &\quad\times\left(\|V_t-V_G\|^{\frac{T_0}{T}+1}-\|V_t-V_G+V_D\|^{\frac{T_0}{T}+1}\right) \end{aligned} \tag{8.4}$$

By using again the Taylor expansion, the current at high gate bias can be approximated by:

$${I_D}^{\mathrm{2D}} \propto (V_{SO}-V_G)^{\frac{T_0}{T}} \tag{8.5}$$

The resulting equation for the current in a monolayer transistor at high gate bias, Eq. 8.5, is again a simple power law, similar to Eq. 8.2. The main difference is in the exponent: T_0/T versus $2T_0/T-1$. The used hopping charge transport description is the same for thick and thin films. However, the carrier confinement results in a qualitatively different temperature dependence. From Eq. 8.5, it is clear that the extrapolated straight line in Fig. 8.3e should, for infinite T, cross the exponent axis at the value 0 instead of -1, which is indeed consistent with the data. From the slope of Fig. 8.3e the values for T_0 can be found. For the SAMFET, we obtain $T_0 = 627$ K and for the T6 monolayer $T_0 = 539$ K. Using the determined values for T_0, the transfer curves as a function of bias and temperature can be fully described using Eq. 8.4. Calculations are presented as solid lines in Fig. 8.3a and c, for the SAMFET and T6 monolayer transistor, respectively. This is the first observation of charge carrier confinement and 2D transport in organic semiconductors.

8.3 Summary

We have analyzed the effect of carrier confinement on the charge transport properties of organic field-effect transistors. Spatial confinement was achieved by the use of semiconductors of which the active layer is only one molecule thick, either by self-assembly or by thermal evaporation. Electrical measurements of the resulting monolayer transistors were compared to measurements of organic transistors with a thick semiconducting polymer as active layer. We have demonstrated that the 2D transport in organic semiconductors is reflected in a reduced temperature dependence of the transfer characteristics.

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Physics of organic ferroelectric field-effect transistors

9

Abstract

Most of the envisaged applications of organic electronics require a non-volatile memory that can be programmed, erased and read electrically. Ferroelectric field-effect transistors (FeFET) are especially suitable due to the non-destructive read-out and low power consumption. In this Chapter, an analytical model is presented that describes the charge transport in organic FeFETs. The model combines an empirical expression for the ferroelectric polarization with the density dependent hopping charge transport in organic semiconductors. Transfer curves can be calculated with parameters that are directly linked to the physical properties of both the comprising ferroelectric and semiconductor materials. A unipolar FeFET switches between a polarized and depolarized state, and an ambipolar FeFET switches between two stable polarized states. A good agreement between experimental and calculated current is obtained. The method is generic; any other analytical model for the polarization and charge transport can be easily implemented and can be used to identify the origin of the varying transconductances reported in the literature.

9.1 Introduction

Most of the envisioned applications of organic electronics require a memory. A non-volatile memory is preferred, that retains its data when the power is turned off, and that furthermore can be programmed, erased and read-out electrically. Ferroelectric field-effect transistors (FeFETs) are attractive for this purpose due to fast non-destructive data read-out and low power consumption [1, 2]. A ferroelectric material exhibits a bistable, remnant polarization that can be switched by electric fields exceeding the coercive field. The layout of a FeFET comprises a metal-ferroelectric-semiconductor layer stack as illustrated in **Fig. 9.1b**, in which the ferroelectric layer serves as the gate dielectric. The ferroelectric layer, because of its remnant polarization, can adopt either of two stable polarization states, which persist when no biases are applied. Switching from one polarization state to the other can occur by applying a gate bias exceeding the coercive field. Depending on the orientation of the polarization, positive or negative charges are induced in the semiconductor at the semiconductor-ferroelectric interface, i.e. in the semiconductor channel. The induced surface charge density shifts the onset of channel accumulation towards either more negative or positive gate bias. Hence, a gate bias window, defined by the shifted onset voltages, exists wherein the drain current may have either of two levels depending on the actual polarization state of the ferroelectric gate dielectric. The corresponding drain current levels can be used to define Boolean '0' and '1' states of a non-volatile memory with non-destructive read-out [2]. The most commonly used organic ferroelectric material in FeFETs is the random copolymer poly(vinylidenefluoride-co-trifluorethylene) (P(VDF-TrFE)), as introduced in Chapter 2. The coercive field is about 60 MV/m and the remnant polarization about 60 $\mathrm{mC/m^2}$ [3, 4].

A typical transfer curve of a unipolar *p*-type FeFET is presented in Fig. 9.1d. Qualitatively the current voltage dependence can be understood as follows. At the beginning of the sweep the ferroelectric is unpolarized. Current starts to flow at the switch-on voltage, here at around a gate bias of 0 V. Upon increasing negative gate bias the ferroelectric polarizes. The drain current gradually increases as a result of both the linear and the ferroelectric polarization. At approximately −20 V the coercive field is reached and the ferroelectric is fully polarized. The ferroelectric polarization is saturated and does not change anymore. A further increase of the gate bias only leads to an increase of the accumulated charge carrier density by the linear polarization. Hence the current hardly increases. Upon scanning back the ferroelectric remains polarized and the current remains high. At a gate bias around 20 V the coercive field is reached and the ferroelectric polarization changes sign. Due to the contacts electrons cannot be injected in the *p*-type semiconductor. The current in the off-state is low. The transistor behaves as a bi-stable memory; at a gate bias of 0 V, the current in the on-state and the off-state differ by more than 4 decades. Details of the device physics however remain elusive. For instance, what is the contribution of the linear and the ferroelectric polarization to the drain current, and is the polarization stable in the off-state? To answer these questions a quantitative analysis is needed, which until now has not been reported for organic FeFETs.

The charge transport in inorganic ferroelectric field-effect transistors has been quantitatively described previously. The ferroelectric polarization was taken into account by an empirical description. Conventional charge transport theory was applied for the inorganic semiconductor. The operation of the FeFET was modeled numerically and a good agreement was obtained [5, 6].

Translating the methodology to organic FeFETs is not straightforward. Contrary to inorganic semiconductors, the charge carrier mobility in organic semi-

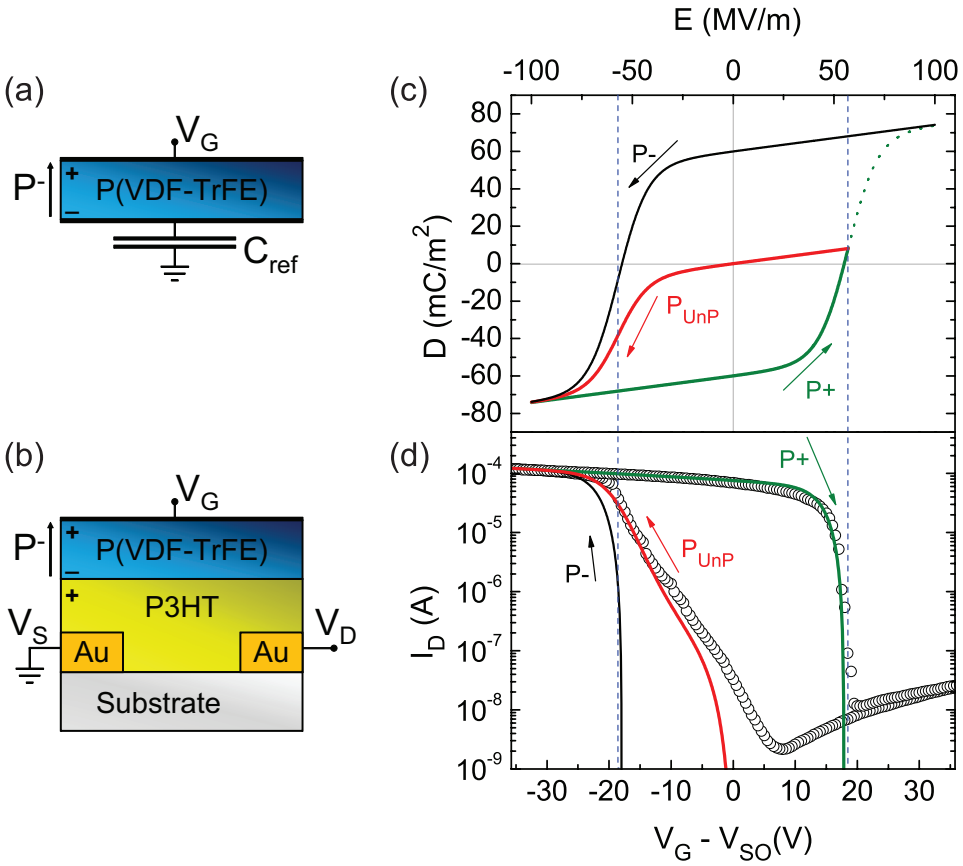

Figure 9.1. (a) Schematic device layout of a ferroelectric capacitor using P(VDF-TrFE) in a Sawyer-Tower circuit. A reference capacitor C_{ref} in series is used to measure the displacement charge. (b) Schematic device layout of a ferroelectric field-effect transistor (FeFET) with P3HT as semiconductor and Au source and drain electrodes. The polarization direction resulting in the high-conductance state is indicated as P^-. (c) Calculated displacement charge of a ferroelectric capacitor as a function of the applied electric field. (d) Linear transfer characteristics of a P3HT FeFET, measured at a drain bias -2 V. The channel length and width were 20 µm and 10 000 µm, and the ferroelectric P(VDF-TrFE) layer thickness was 325 nm. Symbols represent experimental data and the solid lines are model predictions. The arrows indicate the scan direction.

conductors depends on carrier density. A full description of both polarization of the organic ferroelectric and charge transport of the organic semiconductor is required. In this Chapter, we adopt an empirical polarization description that has been successfully used to describe inorganic ferroelectrics. We apply the method to the organic ferroelectric capacitor. With three parameters we can describe the polarization of the capacitor as a function of bias and history.

In order to describe the charge transport of an organic FeFET, an analytical description of the charge transport in the organic semiconductor is needed. We use the model for charge transport based on variable range hopping of charge carriers in an exponential density of localized states, as described in Chapter 3 [7]. The transport is determined separately in non-ferroelectric, conventional organic field-effect transistors as a function of applied bias and temperature. The transport is quantitatively described with parameters that are directly linked to the physical properties of the semiconductor such as the width of the density of states. We combine the polarization and charge transport descriptions into an analytical, physically-based, DC model for organic FeFETs. A good agreement between experimental and calculated transfer curves is obtained. The differences are discussed. We note that the method is generic, any other analytical model for the polarization and charge transport can be implemented.

9.2 Results and discussion

The following Section presents the first ingredient to model the charge transport in organic FeFETs: the description of the polarization behavior in discrete ferroelectric capacitors as a function of applied field and history. With four parameters we can fully describe the electrical displacement. Subsequently, the charge transport in the bare semiconductor is investigated in conventional field-effect transistors as a function of applied bias and temperature. The transport is quantitatively described by a standard hopping model, with parameters that are directly linked to the physical properties of the semiconductor. Then, we combine the two descriptions into a unified analytical model for organic FeFETs. Finally, the current in both unipolar and ambipolar FeFETs is calculated and compared with the experimental data to test and verify the model.

Ferroelectric polarization

The input for modeling the charge transport in an organic FeFET is an electrical description for the polarization of the ferroelectric gate dielectric. Therefore we fabricated capacitors of P(VDF-TrFE) and measured the electric displacement as a function of electric field. The displacement D is the sum of the linear dielectric polarization and the ferroelectric polarization and is given by:

$$D = \varepsilon_0 \varepsilon_F E + P(E) \tag{9.1}$$

where ε_0 is the vacuum permittivity, ε_F the relative permittivity, E the electric field over the ferroelectric and P the ferroelectric polarization. Figure 9.2 shows the

displacement for increasing values of the maximum applied electric field. We start from an unpolarized ferroelectric. When the applied field remains much lower than the coercive field, only the linear dielectric polarization contributes (green triangles). The displacement is symmetric and the lack of hysteresis indicates that there is no ferroelectric polarization. The relative permittivity, ε_F, was determined as 16 in good agreement with literature values [8]. Upon increasing the maximum applied electric field up to the coercive field, E_C, the inner displacement loops shows hysteresis (red circles). The ferroelectric polarization increases with maximum electric field, until the polarization and the hysteresis loop saturate (blue line). The maximum amount of polarization within the ferroelectric, P_S, has been reached (black squares). At zero applied field a remnant polarization P_R remains, which is constant in time as long as depolarization can be disregarded.

We use a reported empirical, analytical description for the saturated and unsaturated polarization as a function of electric field [5, 6]. We start with an unpolarized ferroelectric. The polarization in the first initial measurement is then given by:

$$P_{UnP}(E) = \frac{P_S}{2}\left(\tanh\left(\frac{E+E_C}{\delta}\right) + \tanh\left(\frac{E-E_C}{\delta}\right)\right) \tag{9.2}$$

with:

$$\delta \equiv 2E_C\left(\ln\left(\frac{1+\frac{P_R}{P_S}}{1-\frac{P_R}{P_S}}\right)\right)^{-1}$$

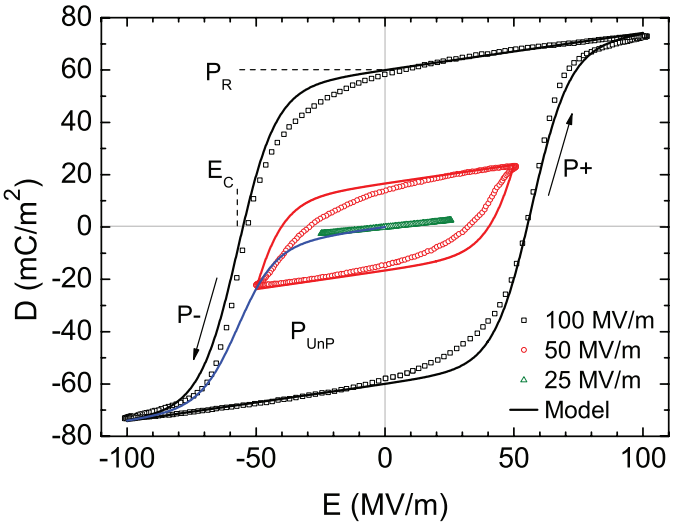

Figure 9.2. Displacement versus applied electric field for a ferroelectric P(VDF-TrFE) capacitor. The scan direction is indicated by the arrows. The displacement was subsequently measured up to 25 MV/m, 50 MV/m and 100 MV/m and presented as the green, red and black dots respectively. The solid lines are fits to the experimental data.

After the first measurement the ferroelectric is partly polarized. The polarization depends on the maximum applied electric field, E_{max}. Subsequent measurements at lower fields change the polarization state of the ferroelectric. These measurements then yield the inner displacement loops. The polarization as a function of field, below the previously applied maximum field is given by:

$$\begin{aligned} P^{+}(E, E_{\max}) &= P_S \tanh\left(\frac{E - E_C}{\delta}\right) \\ &\quad + \frac{P_S}{2}\left(\tanh\left(\frac{E_{\max} + E_C}{\delta}\right) - \tanh\left(\frac{E_{\max} - E_C}{\delta}\right)\right) \end{aligned} \tag{9.3}$$

$$\begin{aligned} P^{-}(E, E_{\max}) &= P_S \tanh\left(\frac{E + E_C}{\delta}\right) \\ &\quad - \frac{P_S}{2}\left(\tanh\left(\frac{E_{\max} + E_C}{\delta}\right) - \tanh\left(\frac{E_{\max} - E_C}{\delta}\right)\right) \end{aligned} \tag{9.4}$$

where P^{-} (P^{+}) denotes polarization towards negative (positive) polarization, as specified in Fig. 9.1b. When the maximum field gets much larger than the coercive field the ferroelectric polarization saturates. The saturated polarization loops follow from Eqs. 9.3 and 9.4 for $E_{max} \gg E_C$ and is given as a function of applied electric field, E, as:

$$P^{+}(E) = P_S \tanh\left(\frac{E - E_C}{\delta}\right) \tag{9.5}$$

$$P^{-}(E) = -P^{+}(-E) \tag{9.6}$$

The displacement loops can be fitted by adding the linear dielectric displacement to the appropriate ferroelectric polarization. The black curve in **Fig. 9.2** is the saturated displacement fitted to the experimental data measured at a maximum electric field of 100 MV/m. A good agreement is obtained using parameter values $P_R = 59.95\,\mathrm{mC/m^2}$, $P_S = 60\,\mathrm{mC/m^2}$, $E_C = 57\,\mathrm{MV/m}$. The values correspond to typical values found for P(VDF-TrFE) capacitors [3, 4, 9, 10]. The measured value of $\varepsilon_F = 16$ was assumed to be frequency and electric field independent. By keeping the four polarization parameters fixed, both the inner loops for the partially polarized ferroelectric and the first initial scan for the unpolarized ferroelectric can be calculated. The blue and red lines are calculated and both show a good description of the experimental data. The differences especially below E_C are due to the simple empirical model used. To derive an improved description is beyond the scope of this work. We note however, that any other analytical formula that yields a better fit can easily be implemented in the charge transport model of the FeFET.

Charge transport in organic transistors

Charge transport in organic semiconductors is governed by thermally activated hopping of charge carriers between localized sites at the Fermi level. The density of the localized states (DOS) can be approximated by a Gaussian or an exponential energy distribution. The Fermi level determines the local occupation of the DOS, i.e. the charge carrier density. With increasing carrier density, hopping becomes more favorable and the mobility increases.

To determine the charge transport properties as a function of carrier density we fabricated separately conventional field-effect transistors of regio-regular poly(3-hexylthiophene) (P3HT), as described in Chapter 2. Standard substrates were used, with SiO_2 as an inert, non-ferroelectric gate dielectric. Linear transfer curves were measured as a function of temperature, and were already presented in Chapter 6, in **Fig. 6.1**. The hysteresis is negligible. The Au source and drain electrodes on P3HT form an ohmic contact for holes resulting in a unipolar *p*-type transistor. At negative gate bias holes are accumulated and the current is enhanced. At positive gate bias the semiconductor is depleted from charge carriers, electrons cannot be injected, and the current is negligible.

The charge transport was described using a model based on variable range hopping in an exponential density of localized states, as presented in Chapter 3 by Eq. 3.12 [7]. Contact resistances and charge trapping are disregarded. For all temperatures a good agreement is obtained.

The transport parameters are below determined in actual FeFETs as well. The possible differences might then be related to changes in physical properties of the semiconductor, such as in the density of states or in the mobility prefactor due to dipolar disorder. We note that we use a standard hopping model. Details such as the influence of deep trap states are not included. However, any other analytical equation that yields an improved description of the charge transport can easily be implemented.

Combined description of a FeFET

In this Section we combine the description for the ferroelectric polarization with that of the charge transport in organic semiconductors. The polarization of the ferroelectric film in a FeFET depends on the electric field over the ferroelectric, induced by the gate bias. We focus on the linear operating regime of the transistor i.e. $|V_G| \gg |V_D|$. We use the gradual channel approximation; the electric field in the direction perpendicular to the channel is much larger than the source-drain field. Hence the electric field is taken to be independent of the position in the channel. We approximate the field by $E = (V_G - V_{SO})/d_F$ where d_F is the thickness of the ferroelectric. The polarization is calculated from the electric field. Depending on the history and scan direction, the applicable description of the ferroelectric polarization, $P(V_G)$ is chosen from Eqs. 9.2–9.6. The polarization corresponds to a surface charge density. As a consequence of Gauss's law, an interface charge at the semiconductor-dielectric interface leads to a shift of the switch-on voltage [11]. Here we include the ferroelectric polarization as a gate-bias-dependent shift of the switch-on voltage. The switch-on voltage V_{SO} used in Eq. 3.12 is therefore replaced

by an effective switch-on voltage, including the polarization:

$$V_{SO}^{pol} = V_{SO} - \frac{P(V_G)}{C_i} \tag{9.7}$$

Introduction of the expression for the effective switch-on voltage combines the descriptions of ferroelectric polarization with the charge transport.

Charge transport in a unipolar FeFET

Unipolar FeFETs were fabricated using P3HT as a *p*-type semiconductor and P(VDF-TrFE) as a ferroelectric gate insulato, as explained in Chapter 3. The linear transfer characteristics are presented in Fig. 9.1d. The gate bias was swept from +35 V to −35 V and back. The ferroelectric layer thickness was 325 nm. Hence the maximum gate field exceeds the coercive field. At the beginning of the sweep the ferroelectric is unpolarized. Upon increasing negative gate bias beyond approximately −20 V, the ferroelectric gets fully polarized. A high hole density is induced at the semiconductor-ferroelectric interface and a high current is measured. Upon scanning back the ferroelectric remains polarized. The current remains high, the FeFET is in the on-state. At a gate bias around +20 V the coercive field is reached and the ferroelectric polarization changes sign. Electron injection into the *p*-type semiconductor is severely hampered due to the use of Au source and drain contacts, as discussed in Chapter 6. The current in the off-state is low.

The question is: is the ferroelectric in the off-state polarized or depolarized? To stabilize the polarization at positive gate bias electrons are required. The electron current is negligible. Hence the ferroelectric polarization cannot be compensated and the ferroelectric depolarizes to the pristine state. The measurement therefore is reproducible; the same drain current loop is measured in a subsequent sweep.

For completeness and to verify the presented methodology, the transfer curves were measured while increasing the maximum negative gate bias from −15 V in steps of −5 V to −50 V. The corresponding linear transfer curves are presented in **Fig. 9.3**. The hysteresis in the drain current increases with maximum applied gate bias until the saturated ferroelectric polarization loop has been reached.

Modeling the charge transport in a unipolar FeFET

By connecting the effective gate bias with the ferroelectric polarization we can calculate the linear transfer curves. Because the polarization depends on the history of applied biases and the applied gate bias, the applicable description of the ferroelectric polarization has to be selected. The parameters describing the polarization, viz. the remnant polarization, saturated polarization, coercive field and relative permittivity, were taken from the fit of the displacement versus field of the P(VDF-TrFE) capacitor as described above (Fig. 9.2): $P_R = 59.95\,\mathrm{mC/m^2}$, $P_S = 60\,\mathrm{mC/m^2}$, $E_C = 57\,\mathrm{MV/m}$, and $\varepsilon_F = 16$. The calculated expected displacement is presented in Fig. 9.1c. The pristine ferroelectric is unpolarized. Upon increasing negative bias the ferroelectric gets polarized (P_{UnP}), and the polarization saturates beyond the coercive field, at a gate bias of about −20 V. On scanning

back, the ferroelectric remains polarized (P^+) up to a gate bias of +20 V, corresponding to the coercive field, where it switches back to the unpolarized, pristine state.

We assume that the remnant polarization (P_R) and the coercive field (E_C) are the same for the ferroelectric in a capacitor and in a transistor. Hence the values determined from the capacitor measurements were used to model the polarization in the FeFET. By including the charge-transport parameters determined from the unipolar P3HT transistor of Fig. 6.1, the transfer curve of the FeFET in Fig. 9.3 can be predicted. However, when using the same values the current in the FeFET is overestimated. To achieve a close fit to the measured FeFET current, an effective mobility of about a factor three lower had to be used. For the optimal fit of Fig. 9.1c–d and Fig. 9.3 we used $\sigma_0 = 6 \times 10^5\,\mathrm{S/m}$, $T_0 = 450\,\mathrm{K}$, $\alpha^{-1} = 2.6\,\text{Å}$, and $V_{SO} = -2\,\mathrm{V}$. The outer, saturated loop is calculated using the description for the unpolarized ferroelectric (P_{UnP}) and the saturated polarization (P^+), presented in Fig. 9.1c–d as the red and green lines, respectively. The same outer curve is shown in Fig. 9.3 as a black line. A good agreement is obtained. The inner current loops of Fig. 9.3 can be calculated as well. Because the applied maximum bias is below the coercive field, the ferroelectric is only partially polarized. Hence for the back scan Eq. 9.3 has to be used, presented as the red, green and blue lines in Fig. 9.3. A reasonable agreement is obtained for the inner loops. The deviations are mainly due to inaccuracies in the simple empirical description of the ferroelectric polarization,

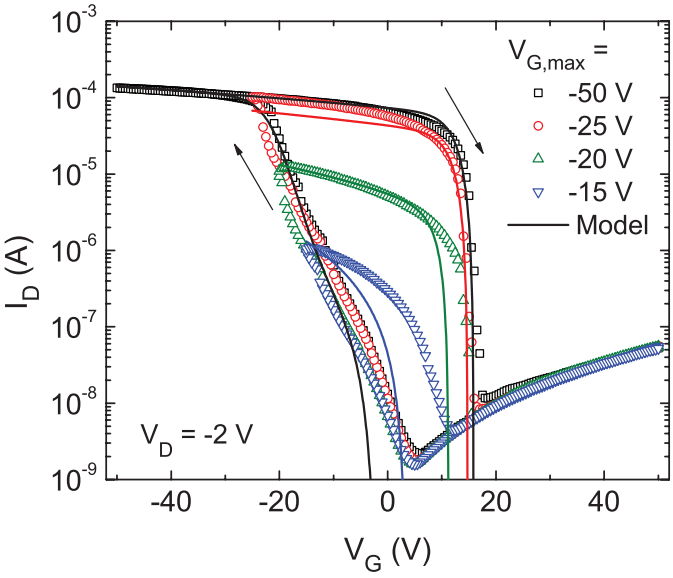

Figure 9.3. Linear transfer curves of a P3HT FeFET. The sweep direction is indicated by the arrows. The gate bias was swept to a maximum negative gate bias from −15 V in steps of −5 V to −50 V, and back to +30 V. The symbols represent the experimental currents and the solid lines are model predictions. The channel width and length were 10 000 µm and 20 µm, and the ferroelectric layer thickness was 325 nm.

especially below the coercive field E_C. To derive an improved description of the inner loop polarization is beyond the scope of this work. We note however, that any other analytical equation that yields a better fit can easily be implemented in the expression for the effective gate bias. Secondly we assume a uniform polarization along the channel. The calculation of the current therefore is only strictly valid for the linear operating regime. Hence, deviations in the saturated and sub-threshold regimes can be expected.

We stress that the ferroelectric switches between a polarized on-state and a depolarized off-state. As an illustration we calculated the current assuming that the off-state is also fully polarized (P^-). The black line in Fig. 9.1c–d shows indeed a striking disagreement with the experimentally measured current.

The effective mobility in the FeFET is a factor of three lower than that in the corresponding conventional transistor. The differences are due to a decreased prefactor and an increased width of the density of states. The increased width of the DOS might indicate dipolar disorder in the FeFET. The decreased prefactor might be due to a field-effect mobility that decreases with increasing dielectric constant [12, 13].

The present description of a FeFET might be used to explain issues reported in literature. In reports on the first FeFETs, it was argued that the ferroelectric polarization in a FeFET is about a factor three lower than in ferroelectric capacitor [14]. However, using the presented model we show that the reduced current in these early FeFETs could be equally due to a lower effective mobility. A definite answer can be given from the analysis of the full temperature dependence. The same holds for reported FeFETs that show large differences in transconductance. For instance the mobility of pentacene [15] and of triisopropyl-silylethynyl pentacene (TIPS-PEN) in FeFETs is reported to be different from that in state-of-the-art regular field-effect transistors [16–18]. The present analytical description might be used to analyze where the differences are coming from.

Modeling the charge transport in an ambipolar FeFET

The first ambipolar ferroelectric transistor was reported in 2005 [19]. As a ferroelectric P(VDF-TrFE) was used and a mixture of poly(2-methoxy-5-(2'-ethylhexyloxy)-p-phenylene vinylene) (MEH-PPV) and (6,6)-phenyl-C_{61}-butyric acid methyl ester (PCBM) as the semiconductor. As source and drain contacts Au was used. Because Au can inject holes in MEH-PPV and electrons in PCBM, ambipolar charge transport was observed. The experimental linear transfer curves are reproduced in **Fig. 9.4**, where the arrows indicate the scan direction. The transfer curve of the ambipolar FeFET shown in Fig. 9.4 exhibits a characteristic 'butterfly' shape: starting in the p-channel mode and scanning to a more positive gate voltage leads to a decrease of the channel (hole) current. When the gate field approaches the coercive field of the ferroelectric, the transistor switches from the p-mode to the n-mode, leading to a sharp decrease and increase in the current. Scanning back to a negative gate bias suppresses the electron current until the hole current switches on. The transistor operates as in a p-type or n-type mode depending on the bias history and has therefore a programmable polarity.

Because both holes and electrons can be accumulated in the channel, both polarization states of the ferroelectric can be compensated. Both polarization states are stable, depolarization can be disregarded. Upon applying gate biases exceeding the coercive field, the ferroelectric switches between the two fully polarized states. To model the ferroelectric polarization we used expressions for the fully saturated polarizations, Eqs. 9.5 and 9.6. We assumed that the remnant and saturated polarization of the ferroelectric are the same as measured in a capacitor. A lower value for the coercive field of $E_C = 40\,\mathrm{MV/m}$ was used. The electron current can be described similar as the hole current (Eq. 3.12) by substituting opposite bias polarities:

$$\begin{aligned} I_D &= f_n \frac{W}{L} \left(\frac{1}{2k_B T_{0,n} \varepsilon_0 \varepsilon_{sc}} \right)^{\frac{T_{0,n}}{T}-1} C_i^{\frac{2T_{0,n}}{T}-1} \frac{T}{2T_{0,n}} \frac{T}{2T_{0,n}-T} \\ &\times \left(\|V_G - V_{SO}\|^{\frac{2T_{0,n}}{T}} - \|V_G - V_{SO} - V_D\|^{\frac{2T_{0,n}}{T}} \right) \end{aligned} \tag{9.8}$$

where the subscript n indicates the electron transport parameters: $T_{0,n}$, $\sigma_{0,n}$, and ${\alpha_n}^{-1}$. To calculate the current we used reported transport parameters for MEH-PPV and PCBM [20, 21]. We only adapted the prefactor for the mobility,$\sigma_{0,n}$. The

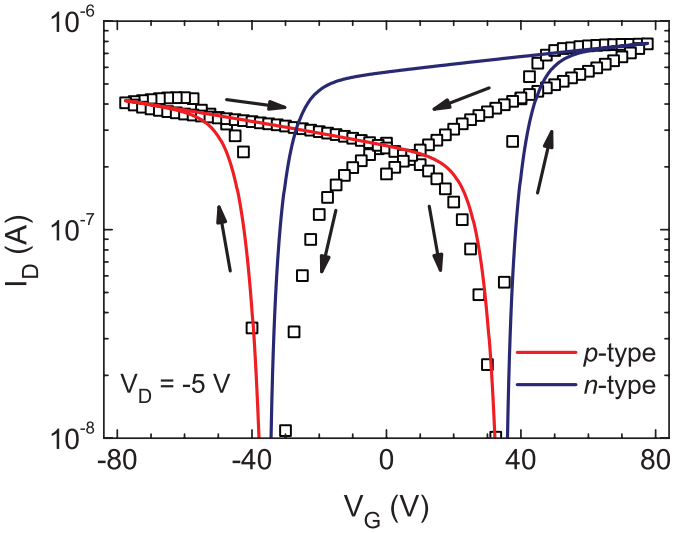

Figure 9.4. Linear transfer curve of an ambipolar FeFET reproduced from Ref. [19] (symbols). A layer of P(VDF-TrFE) with a thickness of 900 nm was used as a ferroelectric gate dielectric. A mixture of MEH-PPV and PCBM was used as the semiconductor. The arrows indicate the scan direction. The solid lines are fits to the experimental data. The transport parameters for the hole transport were: $\sigma_{0,p} = 1 \times 10^5\,\mathrm{S/m}$, $T_{0,p} = 540\,\mathrm{K}$, ${\alpha_p}^{-1} = 1.4\,\text{Å}$. For the electron transport $\sigma_{0,n} = 4 \times 10^5\,\mathrm{S/m}$, $T_{0,n} = 400\,\mathrm{K}$, ${\alpha_n}^{-1} = 1.05\,\text{Å}$. The switch-on voltage was fixed at 0 V.

calculated current is presented by the solid red curve in Fig. 9.4. A good agreement is obtained. We note however that the used prefactor is two orders of magnitude lower than the reported prefactor. This means that the charge transport in the reported ambipolar FeFET is hampered by the un-optimized device processing. P(VDF-TrFE) is a semi-crystalline polymer, hence un-optimized processing yields rough films. The roughness of the ferroelectric gate is directly related to a lower field-effect mobility, as reported in literature [22]. Irrespective of the discrepancies, the analysis clearly shows that the ferroelectric in an ambipolar transistor switches between two stable polarized states.

9.3 Summary

We have presented an analytical model to describe the charge transport in organic FeFETs. Key elements are an empirical reported method to describe the polarization in ferroelectric capacitors and a separate description of the charge transport in organic semiconductors. Upon connecting the effective gate bias with the ferroelectric polarization, the transfer curves in organic FeFETs could analytically be calculated. For both unipolar and ambipolar FeFETs a good agreement has been obtained with parameters that are directly linked to the physical properties of both the comprising ferroelectric and semiconductor materials. Differences are mainly due to the simple empirical model for the polarization. However, any other analytical model for the polarization and for the charge transport can easily be implemented. A unipolar FeFET switches between a polarized and a depolarized state, and an ambipolar FeFET switches between two stable polarized states. The model can be used to identify the origin of the different transconductances reported in the literature. The present model calculates the direct current for a discrete FeFET. It can be directly extended to an AC model that can be implemented in standard circuit simulators to design ferroelectric memory arrays.

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Summary

In our every-day life we find electronic circuits all around us. Of course they can be found in phones and computers but these circuits also control your coffee machine or store the PIN code on your credit card. There is a tendency towards 'smarter' products: train tickets are being replaced by electronic tickets, and bar codes by so-called RFID tags. Making a product 'smart' implies the integration of some kind of electronics. Conventionally, electronic devices and circuits rely on inorganic semiconductors such as germanium and silicon. These materials are robust and can be patterned to form extremely small devices, but they are also expensive and brittle.

Organic electronics on the other hand is based on organic, carbon-based, semiconductors. Organic materials, such as the plastics used to make toys or shopping bags, are usually associated with electric insulation. However, conjugated materials, a special family of organic compounds, have semiconducting properties. The properties of organic materials can be tuned with chemistry, opening a whole new range of possibilities for applications and science. Organic materials can for example be designed to be flexible or soluble in solvents, which allows for flexible electronics and 'ink-based' processing techniques. Additionally, when produced in high volumes, production costs are possibly low. Organic semiconductors are already widely used in organic light-emitting diode (OLED) displays in smart phones. Other envisioned applications of organic semiconductors are flexible organic solar cells and organic electronics.

Electronic circuits are made by combining a large number of transistors. For the progress of organic electronics a thorough understanding of its basic building block, the organic field-effect transistor (OFET), is essential. An OFET acts as a micro-electronic switch: the electrical current between two electrodes depends on the voltage applied to a third electrode. The first two electrodes, the source and drain, are connected to an organic semiconductor. The third electrode is called the gate and is electrically insulated from the semiconductor. The density of mobile charges in the semiconductor is controlled by the gate bias. These charges can move under influence of an electric field between source and drain, resulting in a current. In this thesis several crucial aspects of the device physics of OFETs are studied: the charge transport in the organic semiconductor, charge injection from the contacts into the semiconductor, and the influence of the transistor geometry on the transport.

The conductivity of an organic semiconductor depends on the charge carrier density and the carrier mobility. The mobility in disordered semiconductors itself dependents on the carrier density as well: at low carrier densities the mobility is nearly constant but at high carrier densities the mobility increases with density. In Chapter 4, the charge-carrier mobility is experimentally probed as a function of carrier density for the organic semiconductor P3HT over a wide density range. The mobility at low, $10^{15}\,\mathrm{cm}^{-3}$ to $10^{16}\,\mathrm{cm}^{-3}$, and high, $10^{18}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$, carrier density is extracted from undoped hole-only diodes and field-effect transistors, respectively. The room temperature mobility is nearly constant at densities below $10^{16}\,\mathrm{cm}^{-3}$, whereas the mobility increases with a power law for densities higher than $10^{18}\,\mathrm{cm}^{-3}$. The mobility at intermediate density is probed by chemically doped Schottky diodes and transistors and unites the low- and high density regimes.

The charge carrier density in an undoped organic semiconductor is extremely low. The injection of charges from the contacts into the semiconductor is therefore essential for the operation of an OFET. The charge injection rate depends primarily on the energetic barrier between the metal and the semiconductor. In an OLED the injection barrier should be below 0.3 eV to achieve bulk limited transport. In contrast, an OFET is much more tolerant for injection barriers. In Chapter 5 it is shown that the origin is image-force lowering of the barrier due to the high electric field at the source contact. We employ two-dimensional (2D) numerical charge transport calculations as a tool to get a thorough understanding of the charge injection in OFETs with a coplanar and a staggered layout. In a coplanar OFET under accumulation the electric field at the source contact progressively increases with increasing gate bias. At low gate bias the source contact limits the injection. However, by increasing the gate bias injection barriers up to 1 eV can be surmounted and extracted parameter values resemble those of the bulk semiconductor. The simulations reproduce the typical S-shaped output curves of OFETs with high injection barriers without any further assumptions. In a staggered OFET the injection is gate-bias enhanced until the accumulated channel, opposite to the source contact, screens the gate bias.

In most OFETs, gold is used as electrode metal because it is stable and inert. Gold forms an ohmic contact for holes with many organic semiconductors, resulting in *p*-type OFETs. The injection barrier for electrons is then larger than 1 eV, for which Chapter 5 predicts severe limiting of the carrier injection. In Chapter 6, the formation of an inversion layer is investigated in organic normally-ON unipolar *p*-type transistors. At positive gate bias the measured current is negligible. The absence of the electron current can either be due to trapping of electrons or due to poor electron injection. By studying the depletion current of unipolar *p*-type transistors based on a deliberately doped organic semiconductor we can disentangle these mechanisms since an inversion layer screens the gate bias. Numerically calculated steady-state currents show in accumulation a good agreement with experimental currents. In depletion agreement can only be obtained by suppressing the electron density, which demonstrates that experimentally no inversion layer is formed. In order to form an inversion layer, the carriers have to be supplied by the electrodes. We estimate the injection time assuming thermionic emission

or diffusion limited injection models as the injection mechanism. For a barrier of 1.7 eV we arrive at an injection time of at least 10^8 s. Hence an inversion layer is not formed because the transistors do not reach thermodynamic equilibrium in the time frame of the experiment.

The last three Chapters focus on the device physics of three specific organic transistor configurations: Dual-gate OFETs, organic monolayer FETs, and organic ferroelectric FETs.

Control of the threshold voltage is valuable for logic and sensing applications. The bias on the second gate in a dual-gate transistor modifies the charge density in the semiconductor, an thereby, effectively sets the threshold voltage. In Chapter 7, the charge carrier distribution in organic dual-gate field-effect transistors is investigated as a function of semiconductor thickness, supported by 2D numerical simulations. When the semiconductor thickness is much larger than the accumulation width, two spatially separated channels are formed. The two channels in combination with different effective mobilities cause a distinct shoulder in the transfer characteristics. In contrast, a dual-gate transistor with a semiconducting monolayer has only a single channel. The charge carrier density, and consequently the mobility, are virtually constant in the monolayer. The current changes monotonically with the applied gate biases, leading to transfer curves without a shoulder.

We continue with monolayer transistors in Chapter 8, by answering the question whether a signature of the spatial carrier confinement in these OFETs can be found in the electrical measurements. Spatial confinement is achieved by the use of semiconductors of which the active layer is only one molecule thick, either by self-assembly or by thermal evaporation. Electrical measurements of the resulting monolayer transistors are compared to measurements of organic transistors with a thick semiconducting polymer as the active layer. We demonstrate that the 2D transport in organic semiconductors is reflected in a reduced temperature dependence of the transfer characteristics.

In Chapter 9, an analytical model is presented that describes the electrical transport in organic ferroelectric FETs (FeFETs). Key elements are an empirical expression for the ferroelectric polarization with the carrier density dependent mobility in organic semiconductors. Transfer curves can be calculated with parameters that are directly linked to the physical properties of both the comprising ferroelectric and semiconductor materials. The model describes both unipolar FeFETs and ambipolar FeFETs, the latter supporting both holes and electrons. A unipolar FeFET switches between a polarized and a depolarized state, and an ambipolar FeFET switches between two stable polarized states. The description can be used to analyze FeFET data consistently and can be easily adapted for use in circuit simulators.

Samenvatting

Overal om je heen vind je elektronische circuits. Natuurlijk in computers en mobiele telefoons, maar ook in je koffiezetapparaat of op je bankpas vind je circuits. Er komen steeds meer 'slimme' producten: treinkaartjes worden vervangen door chipkaarten en streepjescodes door draadloze 'RFID-tags'. Deze producten worden 'slimmer' gemaakt door elektronica te integreren. De meeste huidige elektronische circuits zijn gebaseerd op traditionele anorganische halfgeleiders, zoals silicium en germanium. Deze materialen zijn robuust en technieken zijn geoptimaliseerd om extreem kleine structuren en chips te vormen. Traditionele halfgeleiders zijn echter ook breekbaar en duur.

Naast anorganische halfgeleiders bestaan er ook organische halfgeleiders, die de basis vormen voor organische elektronica. Organische materialen zijn op koolstof gebaseerd. Voorbeelden uit ons dagelijkse leven zijn de plastics die gebruikt worden in speelgoed en boodschappentassen. Deze materialen worden meestal geassocieerd met elektrische isolatie, maar een speciale familie onder de organische stoffen, de geconjugeerde materialen, hebben halfgeleidende eigenschappen. Door de eigenschappen van deze stoffen met behulp van scheikunde aan te passen, wordt een scala aan mogelijkheden voor toepassingen en wetenschap toegankelijk. Flexibele materialen maken flexibele elektronica mogelijk en de oplosbaarheid van materialen brengt 'inkt-gebaseerde' fabricagetechnieken dichterbij. Verder kunnen de productiekosten mogelijk sterk verminderd worden indien er op grote schaal geproduceerd wordt. Organische halfgeleiders worden al op grote schaal toegepast in displays gebaseerd op organische lichtuitzendende diodes (OLED's), die je vindt in moderne smartphones. Andere mogelijke toepassingen zijn flexibele organische zonnecellen en organische elektronica.

Om de organische elektronica verder te ontwikkelen is een grondig begrip van de fundamentele bouwsteen essentieel. Deze bouwsteen is de organische veldeffect transistor (OFET), waarvan er een groot aantal gecombineerd kunnen worden tot een elektronisch circuit. Een OFET gedraagt zich als een micro-elektronische schakelaar: de elektrische stroom tussen twee elektrodes hangt af van de aangelegde spanning op een derde elektrode en kan daarmee dus aan- en uitgezet worden. De eerste twee elektrodes, de 'source' en 'drain', zijn aangesloten op een organische halfgeleider. De derde elektrode, de 'gate', is elektrisch geïsoleerd van de halfgeleider. De aangelegde spanning op de gate regelt de dichtheid van mobiele ladingen in de halfgeleider, waardoor een geleidend kanaal gevormd kan worden. De ladingen in het kanaal bewegen vervolgens onder invloed van het elektrische veld tussen de source en drain waardoor er een stroom gaat lopen. Dit proefschrift behan-

delt een aantal cruciale aspecten van de natuurkundige werking van deze OFET's, namelijk het ladingstransport in de organische halfgeleider, de ladingsinjectie van de contacten naar de halfgeleider en de invloed van de transistorgeometrie op het ladingstransport.

Het ladingstransport (de geleiding) in een organische halfgeleider hangt af van de dichtheid en de mobiliteit van de ladingsdragers. Organische halfgeleiders hebben een wanordelijke structuur, waardoor de mobiliteit ook afhankelijk is van de ladingsdragerdichtheid. Voor lage dichtheden is de mobiliteit nagenoeg constant, maar voor hoge dichtheden neemt de mobiliteit sterkt toe met toenemende dichtheid. In Hoofdstuk 4 wordt de mobiliteit in de organische halfgeleider P3HT experimenteel gemeten als functie van de ladingsdichtheid over een groot dichtheidsbereik. De mobiliteit voor lage, $10^{15}\,\mathrm{cm}^{-3}$ to $10^{16}\,\mathrm{cm}^{-3}$, en hoge, $10^{18}\,\mathrm{cm}^{-3}$ to $10^{20}\,\mathrm{cm}^{-3}$, ladingsdragerdichtheid wordt afgeleid van respectievelijk niet-gedoteerde diodes en OFET's. De mobiliteit bij kamertemperatuur is vrijwel constant voor dichtheden lager dan $10^{16}\,\mathrm{cm}^{-3}$, terwijl de mobiliteit met een machtsverband toeneemt voor dichtheden hoger dan $10^{18}\,\mathrm{cm}^{-3}$. De mobiliteit bij tussenliggende dichtheden is bepaald door Schottky-diodes en OFET's chemisch te doteren, door deze bloot te stellen aan een oxiderend gas. Dit levert een totaalbeeld op van lage tot hoge dichtheidsregimes.

De ladingsdragerdichtheid in een niet-gedoteerde zuivere organische halfgeleider is extreem laag. Daarom is de injectie van ladingsdragers vanuit de contacten in de halfgeleider extreem belangrijk voor de werking van OFET's. De mate van injectie hangt voornamelijk af van de energetische barrière tussen het metaal en de halfgeleider. In een OLED moet deze barrière kleiner zijn dan 0.3 eV voor bulkgelimiteerd transport. OFET zijn echter veel toleranter voor injectiebarrières. Hoofdstuk 5 laat zien dat de barrière aanzienlijk verlaagd wordt door de spiegelladingspotentiaal en een hoog elektrisch veld aan het sourcecontact. Om inzicht te krijgen in de ladingsinjectie gebruiken we tweedimensionale numerieke ladingstransportberekeningen. In het hoofdstuk worden zowel coplanaire OFET's als 'staggered' OFETS behandeld. Bij het eerste type bevinden de contacten zich aan dezelfde kant van de halfgeleider als de gate, terwijl bij het tweede type de contacten juist tegenover de gate liggen. In een coplanaire OFET in accumulatie neemt het elektrische veld aan het source contact toe met toenemende aangelegde spanning op de gate. Bij een lage gate spanning limiteert het source contact de injectie van ladingsdragers en daarmee ook de stroom. Bij hoge gate spanning kunnen echter barrières tot 1 eV overwonnen worden en benaderen de afgeleide parameters de bulk halfgeleider waarden. Zonder verdere aannames reproduceren de simulaties de typische S-vorm in de gemeten curves van contactgelimiteerde OFET's. In 'staggered' OFET's wordt de injectie verbeterd door de gate spanning totdat het geaccumuleerde kanaal tegenover het sourcecontact de gate spanning afschermt.

In de meeste OFET's wordt goud gebruikt als elektrodemetaal, omdat het stabiel en niet-reactief is. Goud vormt ohmse contacten voor positieve ladingsdragers met veel organische halfgeleiders, waardoor er *p*-type OFET's ontstaan. De injectiebarrière voor elektronen is dan groter dan 1 eV, waarvoor Hoofdstuk 5 zware belemmering van de elektroneninjectie voorspelt. In Hoofdstuk 6 gaan we hier verder op in en bestuderen het vormen van een zogenaamde inversielaag, een laag elek-

tronen, in organische p-type OFET's. Voor positieve gate spanning is de gemeten stroom verwaarloosbaar. Het uitblijven van een elektronenstroom kan veroorzaakt worden door slecht elektronentransport in de halfgeleider, maar ook door injectiebelemmering van elektronen aan het contact. We kunnen onderscheid maken tussen beide mechanismen door de depletiestroom te meten van p-type OFET's met een opzettelijk gedoteerde organische halfgeleider, omdat een inversielaag hierin de gatespanning afschermt.

Numeriek berekende evenwichtsstromen beschrijven in accumulatie de experimentele stromen uitstekend. In depletie kan alleen overeenstemming bereikt worden wanneer de elektronendichtheid onderdrukt wordt. Dit toont aan dat er experimenteel geen inversielaag gevormd wordt. Om een inversielaag te vormen, moeten de vereiste elektronen geïnjecteerd worden vanuit de contacten. We schatten de benodigde injectietijd met thermionische emissie en diffusiegelimiteerde injectiemodellen als injectiemechanisme. Voor een barrière van 1.7 eV berekenen we een injectietijd van ten minste 10^8 s. Er wordt dan geen inversielaag gevormd, omdat de OFET's geen thermodynamisch evenwicht bereiken op deze tijdschaal.

De laatste drie Hoofdstukken richten zich op de natuurkundige werking van drie specifieke OFET-configuraties: organische FET's met twee gate elektrodes (dual-gate OFET's), organische monolaag FET's en organische ferro-elektrische FET's.

Het kunnen beï nvloeden van de drempelspanning van transistors is waardevol, bijvoorbeeld in toepassingen in digitale circuits en sensors. De spanning op de tweede gate in een 'dual-gate' transistor beïnvloedt de ladingsdichtheid in de halfgeleider en stelt daarmee de drempelspanning in. In Hoofdstuk 7 wordt de ladingsdragerdichtheid in organische dual-gate FET's onderzocht als functie van de halfgeleiderdikte, ondersteund door tweedimensionale numerieke simulaties. Als de halfgeleiderdikte veel groter is dan de accumulatiedikte, ontstaan er twee ruimtelijk gescheiden kanalen. De twee kanalen, in combinatie met verschillende effectieve mobiliteiten, zorgen voor een onmiskenbare 'schouder' in de stroomkarakteristieken. Een dual-gate OFET met een monolaag halfgeleider daarentegen, waarin de actieve laag slechts één molecuul dik is, heeft slechts een enkel kanaal. De ladingsdichtheid, en daarmee ook de mobiliteit, is vrijwel uniform in de monolaag. De stroom verandert monotoon met de aangelegde gate spanningen, wat leidt tot stroomkarakteristieken zonder schouder.

In Hoofdstuk 8 gaan we verder met de monolaag OFET's, door antwoord te geven op de vraag of er in de stroomkarakteristieken een aanwijzing van het ruimtelijk opsluiten van ladingsdragers terug te zien is. Ruimtelijke opsluiting wordt bereikt door het gebruik van halfgeleiders waarvan de actieve laag slechts één molecuul dik is, gemaakt door zelf-assemblage of thermisch opdampen. Elektrische metingen van de resulterende monolaag OFET's zijn vergeleken met OFET's met een polymeerlaag van enkele tientallen nanometers dik als halfgeleider. We laten zien dat het tweedimensionale transport in organische halfgeleiders terug is te zien in een verminderde temperatuursafhankelijkheid in de stroomkarakteristieken.

Een OFET kan als geheugenelement gebruikt worden door het standaard diëlektricum te vervangen door een ferro-elektrische gate-isolator. In Hoofdstuk 9 wordt een analytisch model ontwikkeld dat het elektrische transport in organische ferro-elektrische FET's (FeFET's) beschrijft. De belangrijkste elementen zijn een empirische uit-

drukking voor de ferro-elektrische polarisatie en de ladingsdragerafhankelijke mobiliteit in organische halfgeleiders. Deze elementen worden aan elkaar gekoppeld via een effectieve drempelspanning. Stroomkarakteristieken kunnen berekend worden met parameters die direct gerelateerd zijn aan natuurkundige eigenschappen van enerzijds het ferro-elektrische materiaal en anderzijds de eigenschappen van de halfgeleider. Het model beschrijft zowel unipolaire FeFET's als ambipolaire FeFET's. In het unipolaire type zorgen enkel gaten of enkel elektronen voor de geleiding, terwijl in het ambipolaire type gaten- en elektronengeleiding samen voorkomt. We gebruiken het model om te laten zien dat een unipolaire FeFET schakelt tussen een gepolariseerde en een gedepolariseerde toestand, en dat een ambipolaire FeFET schakelt tussen twee stabiele polarisatietoestanden. De beschrijving kan gebruikt worden om FeFET-metingen consistent te analyseren en kan eenvoudig aangepast en uitgebreid worden voor gebruik in circuitsimulatiesoftware.

Publications

The work presented in Chapters 4–9 is based on the following publications:

- **J. J. Brondijk**, W. S. C. Roelofs, S. G. J. Mathijssen, A. Shehu, T. Cramer, F. Biscarini, P. W. M. Blom, and D. M. de Leeuw, *Two-dimensional charge transport in disordered organic semiconductors*, accepted for publication in Physical Review Letters **2012**.
- **J. J. Brondijk**, F. Torricelli, E. C. P. Smits, P. W. M. Blom, and D. M. de Leeuw, *Gate-bias assisted charge injection in organic field-effect transistors*, Organic Electronics 13, 1526 **2012**.
- **J. J. Brondijk**, M. Spijkman, F. van Seijen, P. W. M. Blom, and D. M. de Leeuw, *Formation of inversion layers in organic field-effect transistors*, Physical Review B, 85, 165310 **2012**.
- **J. J. Brondijk**, M. Spijkman, F. Torricelli, P. W. M. Blom, and D. M. de Leeuw, *Charge transport in dual-gate organic field-effect transistors.* Applied Physics Letters 100, 023308 **2012**.
- **J. J. Brondijk**, K. Asadi, P. W. M. Blom, and D. M. de Leeuw, *Physics of organic ferroelectric field-effect transistors.* Journal of Polymer Science Part B: Polymer Physics 50, 47 **2012**.
- **J. J. Brondijk**, F. Maddalena, K. Asadi, H. J. van Leijen, M. Heeney, P. W. M. Blom, and D. M. de Leeuw, *Carrier-density dependence of the hole mobility in doped and undoped regioregular poly(3-hexylthiophene).* Physica Status Solidi B 249, 138 **2012**.

Other publications:

- M. Spijkman, **J. J. Brondijk**, T. C. T. Geuns, E. C. P. Smits, T. Cramer, F. Zerbetto, P. Stoliar, F. Biscarini, P. W. M. Blom, and D. M. de Leeuw, *Dual-Gate Organic Field-Effect Transistors as Potentiometric Sensors in Aqueous Solution.* Advanced Functional Materials 20, 898 **2010**.
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- **J. J. Brondijk**, X. Li, H. B. Akkerman, P. W. M. Blom, and B. de Boer, *Microcontact printing of self-assembled monolayers to pattern the light-emission of polymeric light-emitting diodes.* Applied Physics A 95, 1 **2008**.

- N. I. Craciun, **J. J. Brondijk**, and P. W. M. Blom, *Diffusion-enhanced hole transport in thin polymer light-emitting diodes.* Physical Review B 77, 035206 **2008**.

- Hee Hyun Lee, **J. J. Brondijk**, N. G. Tassi, S. Mohapatra, M. Grigas, P. Jenkins, K. J. Dimmler, and Graciela B. Blanchet, *Direct printing of organic transistors with 2 μm channel resolution.* Applied Physics Letters 90, 233509 **2007**.

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Auke, vanaf ons afstuderen zijn wij roomies geweest, van de kelder via de eerste verdieping naar de begane grond. Door je brede wetenschappelijke interesse en kennis hebben we vele interessante discussies gehad, al is de appendix met uitleg over de DVD en 3D-film er bij mij ook niet van gekomen. Boven alles hebben we

een ontzettend leuke tijd gehad en veel cools meegemaakt. Onder andere een road trip zonder BMW's maar met een dikke Dodge. Naast Steel Panther zal ik ook nooit vergeten hoe je rigoureus de wat softere nummers uit de Rolling Stone 500 kon deleten. Heel gaaf dat je mijn paranimf wil zijn.

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